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Survey paper on multiplier-less 1-D discrete wavelet transform based on NEDA technique

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Abstract

Traditional disseminated math (DA) is well known in field programmable entryway cluster (FPGA) plan, and it includes on-chip ROM to accomplish fast and normality. In this paper, we portray fast zone proficient 1-D discrete wavelet change (DWT) utilizing 9/7 channel based new effective dispersed number juggling (NEDA) Technique. Being region productive design free of ROM, increase, and subtraction, NEDA can likewise uncover the repetition existing in the snake exhibit comprising of sections of 0 and 1. This design underpins any size of picture pixel esteem and any level of decay. The parallel structure has 100% equipment usage effectiveness.

Keywords

1-D Discrete wavelet transform (DWT), NEDA, Low pass filter, High pass filter, Xilinx simulation.

1.Introduction

The outstanding picture coding models, in particular, MPEG-4 and JPEG2000 have embraced 1-D DWT as the change coder because of its surprising points of interest over alternate changes. For lossy and lossless pressure, Daubechies 9/7 orthogonal channel is utilized as the default wavelet channel in JPEG 2000. Proficient usage of 1-D DWT utilizing 9/7 channels in asset compelled hand-held gadgets with capacity for ongoing preparing of the calculation serious mixed media applications is, accordingly, an important test. Multiplier-less equipment usage approach gives a sort of answer for these issues because of its extension for bring down equipment many-sided quality and higher throughput of calculation.

A few parallel and pipeline frameworks that meet the computational necessities of the discrete wavelet change have been proposed. Some of them require multiprocessor to execute it and the framework is perplexing, tedious, and exorbitant [1]. The Field programmable entryway cluster (FPGA) gives us another approach to advanced flag preparing [2].

A few plans have been proposed for the multiplier, multiplier-less usage of 1-D DWT in view of the guideline of multiplier based outline (MBD) circulated number juggling (DA) canonic marked digit (CSD), [1]– [3]. The structure of circulates the bits of the settled coefficients rather than the bits of information tests. Thusly, the snake many-sided quality of the structure of relies upon the DA-framework of the settled coefficients [2].

Canonic marked digits (CSD) are mainstream for speaking to a number with least number of non-zero digits. The CSD portrayal of a number contains the base conceivable number of nonzero bits, along these lines the name canonic. The CSD portrayal of a number is novel and CSD numbers cover the range (-4/3, 4/3), out of which the incentive in the range {-1, 1} are of most prominent intrigue.

Martina et al [5] have approximated the 9/7 channel coefficients and execution of an equipment usage of the 9/7 channel bank relies upon the precision of coefficients portrayal. By that approach, they have fundamentally lessened the snake many-sided quality of the 9/7 DWT. Gourav et al [7] have proposed a LUT-less DA-based outline for the usage of 1-D DWT. They have wiped out the ROM cells required by the DA-based structures at the cost of extra adders and multiplexors.Some of them need Rom to implement it and the system is complex, time consuming, and costly [4] The adder-complexity of this structure is significantly higher than the other multiplier-less structures. In this paper, we have proposed an efficient scheme to derive NEDA-based bit-parallel structures, for low-hardware and high-speed computation DWT using 9/7 filters [4].

The remainder of the paper is organized as follows: New efficient distributed arithmetic based computation of 1-D DWT using 9/7 filter is presented in Section II. The proposed structures are presented in Section III. Hardware and time complexity of the proposed structures are discussed and compared with the existing structures in Section IV. Conclusion is presented in Section V.

2.New efficient distributed arithmetic (NEDA)

Let us consider the following sum of products [4]:

$$R = \sum_{k=1}^{L} X_k \times Y_k \qquad (1)$$

Where X_k are fixed coefficients and they Y_k are the input data words. Equation (1) can be expressed in the form of a matrix product as:

$$R = [X_1 \quad X_2 \quad \ldots \quad X_L] \begin{bmatrix} Y_1 \\ Y_2 \\ . \\ Y_L \end{bmatrix} \qquad (2)$$

Both X_k and Y_k are in two's complement format. The two's complement representation of X_k may be expressed as

$$X_k = -X_k^M 2^M + \sum_{i=N}^{M-1} X_k^i 2^i \qquad (3)$$

Where $X_k^i = 0$ or 1, and $i =$ N, N+1… M and X_k^M is the sign bit and X_k^N is the least significant bit (LSB).

Equation (3) can be expressed in matrix form as:

$$X_k = \left[2^N \quad 2^{N+1} \quad \ldots \quad 2^M\right] \begin{bmatrix} X_k^N \\ X_k^{N+1} \\ . \\ -X_k^M \end{bmatrix} \qquad (4)$$

Similarly Y_k can be represented in two's complemented format as:

$$Y_k = -Y_k^X 2^X + \sum_{i=W}^{X-1} Y_k^i 2^i \qquad (5)$$

Where $Y_k^i = 0$ or 1, and $i =$ W, W+1, …,X and Y_k^M is the sign bit and Y_k^N is the least significant bit (LSB).

Now on combining equations (1) and (3), we get-

$$R = -(R^M.2^M) + \sum_{i=N}^{M-1}(R^i.2^i) \qquad (6)$$

Where

$$R^i = \sum_{k=1}^{L} X_k^i Y_k \,, \; i = \text{N, N+1} \ldots \text{M}$$

3.Proposed architecture

In this paper, we have proposed a high speed area efficient multiplier-less 1-D 9/7 wavelet filters based NEDA technique. 9/7 wavelet filters coefficient i.e. 9 low-pass and 7 high-pass wavelet filters coefficient are given in table1. We multiply the filter coefficients by 128 for simplification. The mathematical calculation for 1-D high pass filter output is explained by an example.

Table 1 Show high-pass and low-pass wavelet filters coefficient

	Wavelet filters coefficients	**Multiplied by 128**	**8 bit binary representation with 2's complement of negative no.**
h_0	0.60294901823	77	01001101
h_1	0.26686441184	34	00100010
h_2	-0.07822326652	-10	11110110
h_3	-0.01686411844	-2	11111110
h_4	0.026748757410	3	00000011
g_0	0.55754352622	71	01000111
g_1	-0.29563588155	-38	01011010
g_2	-0.02877176311	-4	11111100
g_3	0.045635881557	6	00000110

Where $h_0, h_1, h_2, h_3,$ h_4 are the Low pass filter coefficients and g_0, g_1, g_2, g_3 are the High pass filter coefficients.

If we take the high pass coefficients g_0, g_1, g_2 and g_3 multiply by r_1, r_2, r_3 and r_4 then we get the High pass output Y_H of the 9/7 filter as [6-10]:

$$Y_H = [g_0 \quad g_1 \quad g_2 \quad g_3] \begin{bmatrix} r_1 \\ r_2 \\ r_3 \\ r_4 \end{bmatrix} \qquad (7)$$

Where

$$r_1 = Y(n) + Y(n-6)$$
$$r_2 = Y(n-1) + Y(n-5)$$
$$r_3 = Y(n-2) + Y(n-4)$$
$$r_4 = Y(n-3)$$

Let r_1=1, r_2=2, r_3=3, r_4=4 then

$$Y_H = [71 \quad -38 \quad -4 \quad 6]\begin{bmatrix}1\\2\\3\\4\end{bmatrix} = 7 \qquad (8)$$

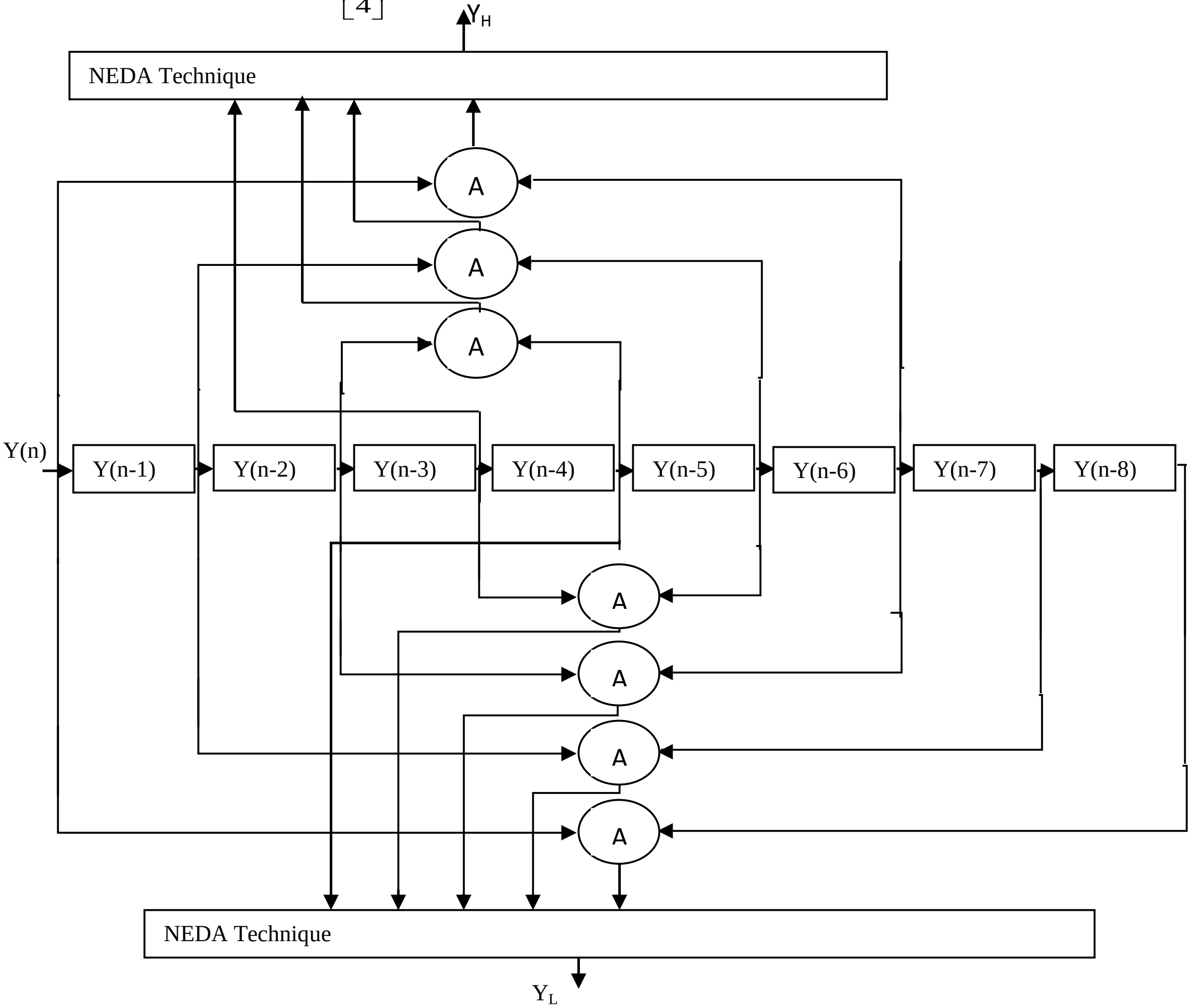

Figure 1 Proposed multiplier-less 9/7 wavelet filter using NEDA technique

Now if we implement this with NEDA then

$$Y_H = [01000111 \quad 11011010 \quad 11111100 \quad 00000110]\begin{bmatrix}r_1\\r_2\\r_3\\r_4\end{bmatrix} \qquad (9)$$

Now we can make the DA matrix by the filter coefficients as

$$[B_k] = \begin{bmatrix}1 & 0 & 0 & 0\\1 & 1 & 0 & 1\\1 & 0 & 1 & 1\\0 & 1 & 1 & 0\\0 & 1 & 1 & 0\\0 & 0 & 1 & 0\\1 & 1 & 1 & 0\\0 & 1 & 1 & 0\end{bmatrix} \qquad (10)$$

$$Y_H = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 \end{bmatrix} \begin{bmatrix} r_1 \\ r_2 \\ r_3 \\ r_4 \end{bmatrix} = \begin{bmatrix} r_1 \\ r_1 + r_2 + r_4 \\ r_1 + r_3 + r_4 \\ r_2 + r_3 \\ r_2 + r_3 \\ r_3 \\ r_1 + r_2 + r_3 \\ r_2 + r_3 \end{bmatrix} \quad (11)$$

In Figure 2, apply NEDA techniques step-1 all the input converts’ binary number, Step-2 all the binary input applied to sign extension, after than all the sign extension input applied to a adder array so,

$P_1 = 00001$, $P_2 = 00111$

$P_3 = 01000$, $P_4 = 00101$

$P_5 = 00101$, $P_6 = 00011$

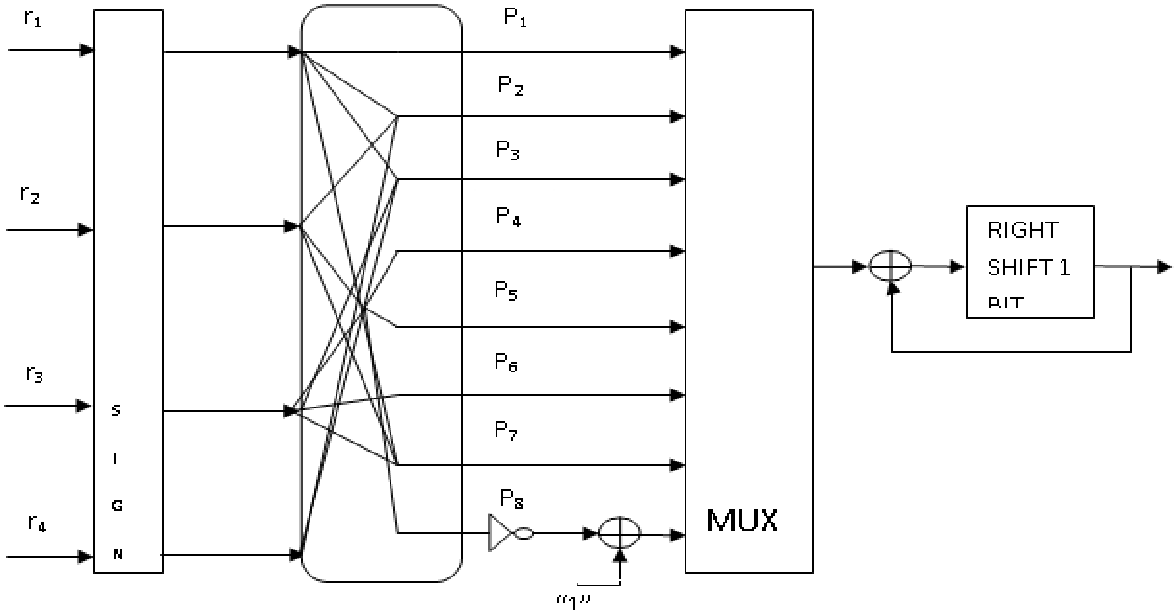

Figure 2 Mathematical calculation of the NEDA technique of the low-pass wavelet filter output

$P_7 = 00110$, $P_8 = 00101$

The entire adder array input applied to MUX so, the entire adder array input $m(1)$ right shift 1-bit so

MUX (1) = 0’0111 = Y_P (0)

MUX (1) add MUX (2) = Y_P (1)
= 0’00001
= 0 0111
+ 0 01111

Output of the Y_P (1) again right shift 1-bit and adds MUX (3) so
= 0’001111
= 0 1000
+ 0 101111

Y_P (1) + MUX (3) = Y_P (2)

Output of the Y_P (2) again right shift 1-bit and adds MUX (4) so
= 0’0101111
= 0 0101
+ 0 1010111

Y_P (2) + MUX (4) = Y_P (3)

Output of the Y_P (3) again right shift 1-bit and adds MUX (5)
so
= 0’01010111
= 0 0101
+ 0 10100111

Y_P (3) + MUX (5) = Y_P (4)

Output of the Y_P (4) again right shift 1-bit and adds MUX (6)
so
= 0’010100111
= 0 0011
+ 0 100000111

Y_P (4) + MUX (6) = Y_P (5)
Output of the Y_P (5) again right shift 1-bit and adds MUX (7)
so

= 0’010000111
= 0 0110
+ 0 1010000111

Y_P (5) + MUX (7) = Y_P (6)
Output of the Y_P (6) again right shift 1-bit and adds MUX (8)
so

= 0’01010000111
= 1 1011
+ 1000000000111

Total output Y_P (7) = 000000000111 = 7
Carry is rejected.

4.Simulation result

The proposed architecture has very low hardware complexity compared to DA based structures, because DA requires ROM. In the proposed architecture, calculate the high-pass and low-pass wavelet filter output using NEDA scheme. NEDA does not require ROM. Proposed structure consist only 33 adders, zero mux and 29 registers. In the proposed architecture is better than other architecture in shown the Table 2.

Table 2 Comparison of proposed with existing architectures Arch.: architecture, MUL:multiplier MUX: multiplex, REG: Register, CP: Cyclic Period

Arch.	MUL	Adder	MUX	Rom	Reg	CP
Alam et al. [2]	0	43	9	4	8	12 T_A
Martina et al [5]	0	36	5	4	8	9 T_A
Martina et al. [6]	0	36	4	4	8	6 T_A
Gaurav et al. [7]	0	30	1	4	8	6 T_A
Proposed	0	30	1	0	8	6 T_A

5.Conclusion

We propose a novel appropriated number-crunching worldview named NEDA for VLSI execution of advanced flag preparing (DSP) calculations including inward result of vectors and vector-grid duplication. Numerical evidence is given for the legitimacy of the NEDA plot. We show that NEDA is an exceptionally effective engineering with adders as the principle part and free of ROM (free memory), duplication, and subtraction. For the viper exhibit, an efficient approach is acquainted with evacuate the potential repetition so least increases are important. NEDA is an exactness protecting plan and fit for keeping up a tasteful execution even at low DA accuracy.

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