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Analysis of low power (SRAM) static random access memory design

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Abstract

In electronics embedded memories requires for a large scale of the overall silicon area and power consumption in modern SoC(s). Current trends on transistor scaling combined with the low-power applications in electronics devices. It increases the chance of susceptibility of VLSI circuits for soft-errors detection, especially exposed to extreme environmental conditions, for space applications. The most exdesignent part of these circuits is memory it covers large areas of the silicon die data storage. Radiation hardening of embedded memory blocks commonly gained for use of extremely large bit designs and for a relatively high operating voltage; however, in additional resulting area overhead, this limits operating voltage of the entire system for significant power consumption. In this paper, we propose the static random access memory (SRAM) bit design uses the low-voltage supply. It proposed 13T dual-driven separated-feedback mechanism to charge deposits as high as 500 fC at a scaled 500-mV supply voltage. The article is achieved with a design layout that is only 2 times larger than 6T SRAM design with standard design rules.

Keywords

Static random access memory (SRAM) , Critical charge, Low voltage, Radiation effects, Radiation hardening, Single-event upset (SEU), Soft errors, Space applications, Sub threshold, Ultralow power (ULP).

1.Introduction

The POWER dissipation on VLSI systems is one of the most important issues for current nanoscale Designing. Ultra low power application is most important in VLSI chips for space applications; natural energy resources are very limited. Low-cost satellites operates in lower power budget, the total weight of satellite is reduced by restricting the use of highly weighted batteries and supplies systems. The most efficient way to achieve low power operation in integrated circuits is to reduced the power supply voltage and operate all components of the chip in threshold region range[1], [2], so we can significantly reduced both static and dynamic power consumption. However, the main challenges is a low-voltage circuit design, like increased delay, sensitivity in the process variations, and continuously temperature fluctuations, Low-voltage circuits susceptible to radiation effects than circuits powered on nominal supply [3].Soft errors or single-event upsets (SEUs) caused by radiation strikes are the primary causes of failure in VLSI circuits operating within a highly radiating environment. Accordingly, maintaining data integrity in light of SEUs has become an integral aspect of memory design [4]. Soft errors occur when an energetic particle hits and passes through a semiconductor material, potentially causing a bit flip in the memory design [5], [6].

2.Review of related work

Very low power consumption in the memory system plays an important role in the VLSI systems designing. But during the operation memory consumes very high power supply. Sub-threshold leakage power is the main drawback for high power Consumption in the systems. *FIN type Field Effect Transistors* in the electronics (FinFET) based 10T SRAM design is designed to reduce the leakage power in CMOS based Static Random Access Memory (SRAM). FinFET used for bulk CMOS in nano scale circuits it effectively reduces the total active power consumption in digital circuits.

In electronics FinFET devices used for reduction in standby power supply which is more suitable for low-power designs while simultaneously providing higher performance [5]. The low power techniques used for FinFET circuits effectively reduces the circuit power. Current trend of the growing demands for high-density logical memories in modern microprocessors and other VLSI System-on-Chip (SoC) designs [1], gain design embedded RAM used as an alternative to static random access memory (SRAM) due to its high-density, non-destructive read operation, low leakage power [2–5]. However, in this technique we requires always periodical refresh cycles operation in selected interval to reliably retain data, both reducing the availability of memory space and consuming dynamic refresh power.

3.SRAM operation

The SRAM has different operation states such as standby, reading and writing. For operation in read and write mode SRAM should have “readability and “write stability” capability respectively.

A. *Standby:* If the word line is not asserted, for continuous power supply operation the two cross coupled inverters formed and it will continue to reinforce each other as long as they are connected to the supply.

B. Reading: The minimum voltage that is attained during read operation is called as read voltage. Read voltage is the division of voltage between pull down transistor and access transistor. Read stability can be established by low access transistor driving strength which decreases the read voltage.

C. Writing: The maximum voltage that is attained during write operation is called as write voltage. The by division of voltage between pull up transistor and access transistor is the write voltage. Write stability can be established by strong access transistor driving strength which decreases write voltage.

D. Clock rate and power: The total consumption of power of SRAM varies in the system it is mostly dependent on how frequently it is accessed, it can be used power hungry as dynamic random access memory (DRAM), when used at high frequency and some ICs consume more watts at full bandwidth [8]. On the other hand, static RAM used at a slower pace, in applications like clocked microprocessors uses very less power and can have nearly negligible power consumption when sitting idle in the region of a few micro watts.

E. Embedded use of SRAM: The Static RAM used as dual ported form it is used for real-time digital signal processing operational circuitry [4]. Many categories like industrial and scientific subsystem, automotive system and electronics contain static random access memory. Several megabytes may be used in complex products such as digital cameras, design phones and synthesizers etc. Static random access memory is also used in personal computers, routers, hard disk buffer etc [8]. LCD screens and printers also normally uses static RAM to hold the image display.

3.1Different sram designs

(I) Conventional 6T SRAM Design

Figure 1 shows the circuit diagram of conventional 6T SRAM[4].this design of SRAM is most simple and less area consumed design it consists of two access transistors and two cross coupled inverters with common read and write port. In case of the write operation the WL is selected, access transistors are turned on; the value to the bit line and bit line bar is given and is stored at q and q-bar.

Before the read mode , the bit lines (BL) and bitbar line(BL bar) are precharged to high as V_{dd} (supply voltage).when the word line is enabled, current will flow from V_{dd} through the pull up transistor TP1of the node storing 1. Simultaneously current will start flow from precharged bitbar line to ground, thus discharging bitbar line. All this causes voltage difference between the bit lines, this voltage difference is detected and amplified with the help of sense amplifiers at the data output.

ADVANTAGES: The SRAM design is very simple, less area consumed and thus it can be used in high density chips.

DISADVANTAGE: on voltage scaling, it has less stability, has high power consumption and high access time requirement.

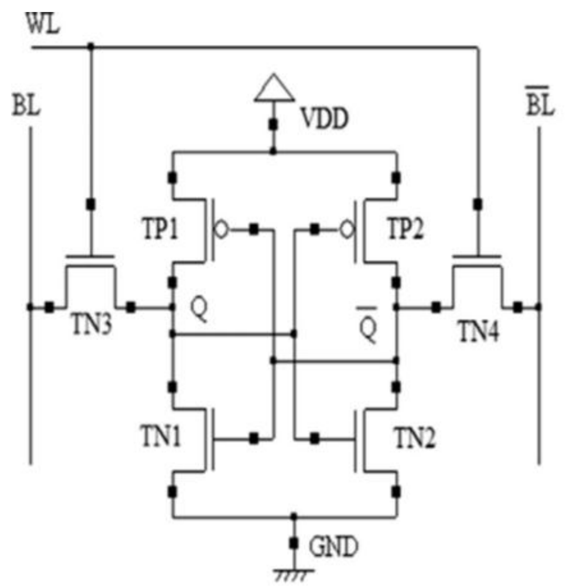

Figure 1 Conventional 6T SRAM Design

(II)High stable, sub-threshold 7T SRAM Design for Ultra –low power application

Figure 2 shows the sub-threshold 7T SRAM [6]. It is sub-threshold 7 transistor based SRAM working on supply base voltage of 0.17V. Like 6T SRAM it has single sided write operation. For the write operation purpose word line (WL) is set high and write bit line is precharged with the data to be stored in the design. Write bit line is precharged higher than the write margin of the design to reduce dynamic power during write 1 operation.

Read path is separated from the storing node of the design which increases noise margin. For reading of the data, Read word line and Read bit both are set to high. Transistors M6, M7 are used for reading the design data. The connection of M7 transistor to virtual ground minimizes the standby leakage of the design.

ADVANTAGES: This design demonstrates 7 times higher dynamic read noise margin compared to the 6T SRAM design. Design also works well in sub-threshold region with low supply voltage as low as 0.17V [6].

DISADVANTAGE: This design has shown increase of area by almost 7% higher than the 6T SRAM.

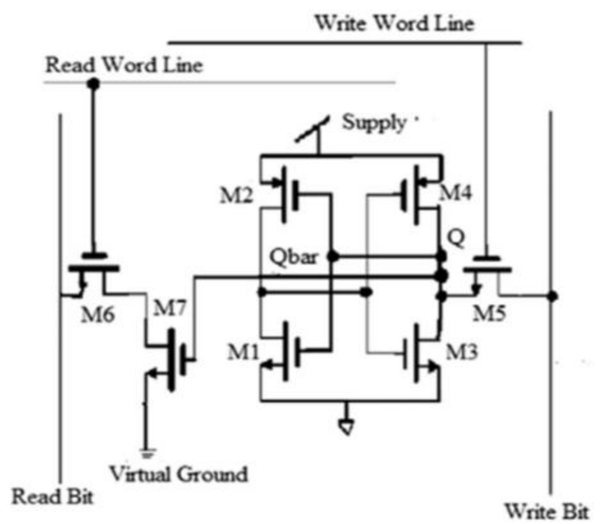

Figure 2 Subthreshold 7T SRAM Design

(III) 9T SRAM Design

Figure 3 shows 9T SRAM [7] which is simulated on 65nm technology. This design is proposed for reducing leakage power and improving data stability of systems. In this design uses two sub-circuits, one the upper sub-circuit which is simply like 6T SRAM design but with minimum sized features. This sub-circuit is used for write operation. Lower sub-circuit consists of access transistors N5 and N6 and one read access transistor N7. Transistor N5 and N6 are controlled by data present on the node 1 and node 2 respectively. However transistor N7 is controlled by read signal RD.

For the write operation purpose, WR signal is set to high, turning the access transistors N3 and N4 ON, while RD set low thus maintaining N7 transistor in cut off mode. Bit lines are than precharged with the data and gets stored on node 1 and node2.

Read operation occurs separately through N5, N6 and N7. During this operation WR is set low while RD set high making transistor N7 in working mode. If node 1 stores '1'data, bit line is discharged through N5 and N7, and when bitbar line stores '1' it gets discharged through N6 and N7, causing in both the cases potential difference between the bitlines which is sensed and amplified by the sense amplifier during this read operation.N3 and N4 are cut-off, thus storage nodes node 1 and node 2 are completely isolated from the bitlines during read operation.

ADVANTAGES: The leakage power consumed by the 9T SRAM design is 7.7% lower as compared to the standard 6T SRAM [7].

DISADVANTAGE: the area consumed by this design is more by 37.8% as compared to the conventional 6T SRAM design and is slightly more than 7T SRAM design [7].

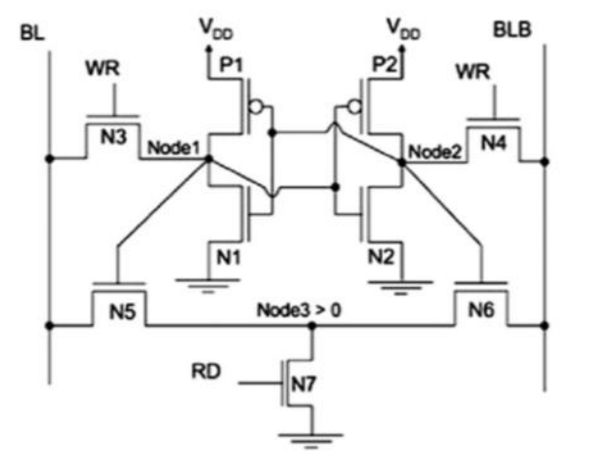

Figure 3 9T SRAM Design

(IV) 10T SRAM Design

Figure 4 shows 10T SRAM for low leakage and sub threshold operation [8]. This can operate at a voltage as low as 285mV [8]. The design consists of two cross coupled P-P-N inverters. Transistors PUL1, PUL2 AND PDL2 form one P-P-N inverter and PUR1, PUR2, PDR2 form another, where PUL stands for pull-up-left ,PUR for pull up right, PUD for pull-down left and PDR for pull down right. Two more transistors pass gate left (PGL) and pass gate right (PGR) are the access transistors controlled by write line WL. For the read operation, discharging path is provided by additional transistors either PDL1 or PDR1. The source terminal of these two transistors is connected to VGND. Whenever the write operation is going VGND is set high to V_{dd} to remove unnecessary leakage current and only during read operation it is connected to ground, giving discharging path to one of the bitlines.

Here Node PQ and pQb are called the pseudo storage nodes, both are used between the two cascaded PMOS's. The presence of these pseudo nodes causes the isolation of the actual storing Nodes from the pair of bit lines which helps to reduce the data-dependent bitline leakage. Rest of the write and read operation is same as that in the 6T SRAM design.

ADVANTAGES: In this design has low power dissipation as compared to 6T SRAM also works better in sub threshold voltage as low as 285Mv[8]

DISADVANTAGE: the area covered by the design is more as more no of transistors are being used in the design as compared to the 6T SRAM design.

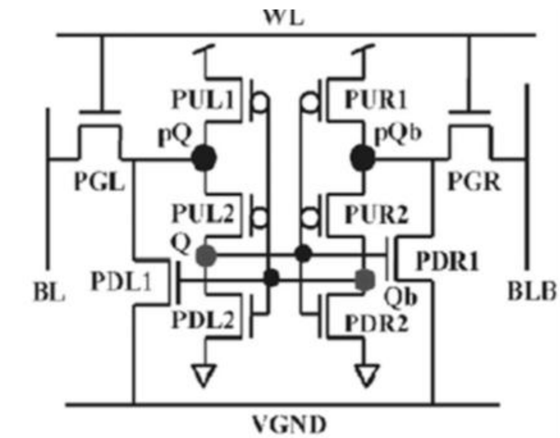

Figure 4 10T SRAM Design

(V) 11T SRAM Design

Figure 5 shows low power 11T SRAM [9]. This design is proposed for low power consumption which has 11 numbers of transistors on 0.25 um technology with the help of tanner EDA tool. Basic storing design of the design is same as that of 6T SRAM with transistors P1, P2, N1, N2, N3 and N4, where N3 and N4 are controlled by word line WWL. In addition to the 6T design there are two tail transistors N7and N9 which are controlled by bit line and bit bar line respectively. Another two transistors N8 and N6 are used for read operation. Transistor N5 is the access transistor for read operation which is driven by read word line RWL. Single bit-line RBL is used for read operation.

During write operation RWL is set low and WWL is select high thus turning access write transistors N3 and N4 on. Bit lines are precharged according to the data to be stored in the design. During read operation WWL=low and RWL= high, thus turning transistor N6 and N8 on. Depending upon the stored data at node B, either read '0' or read '1' can be performed.

ADVANTAGES: The proposed SRAM design consumes approximately 40% less average power compared to conventional 6T SRAM design [9].

DISADVANTAGES: The proposed design consumes more are than the 6T SRAM as well as this design is almost 7% slower than the conventional design during the write operation due to two tail transistors [9].

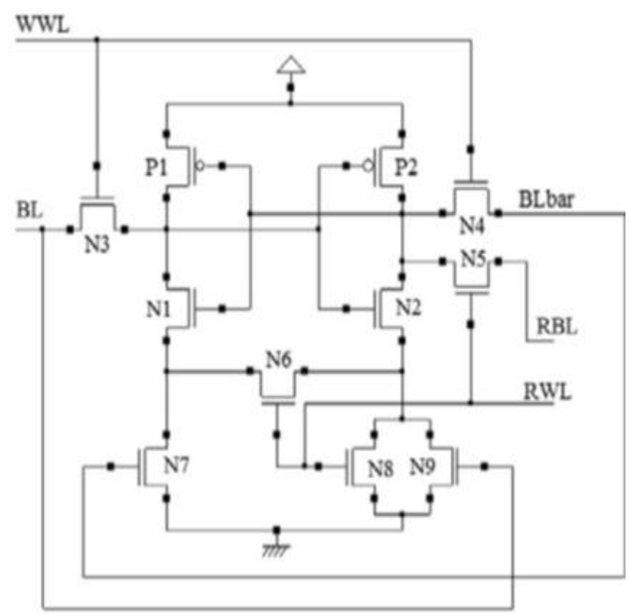

Figure 5 11T SRAM Design

(VI) 12T SRAM Design

Figure 6 shows the design of low swing and multi threshold voltage based low power 12T SRAM [10-12]. This design is proposed mainly for the low power application and is simulated on 45 nm technology. The read and write operation of the design is exactly the same as that of 6T SRAM. As it includes 6T SRAM along with some extra circuitry for low power dissipation in the design.

This design makes use of two voltage sources V1, connected to the bitline through transistor VT1 and V2, connected to the bitbar line through transistor VT2 which reduce the swing at the output node and thus reduce the dynamic power dissipation of the design during the switching activity. Transistor VT1 and VT2 are controlled by data precharged to the bitline and bitbar line respectively. whenever the bitline ='1' and bitbar line ='0', transistor VT1 is turned on and VT1 turned off. Thus forcing the voltage swing to decrease at the output node of the bit line. Similarly for the write operation of '0' reverse case occurs and transistor VT2 is on thus voltage source V2 forces decrease of the swing voltage at node connected to bitbar line.

Thus in both cases decreases the dynamic power of the design. As the design is making use of low V_t transistors (of inverter) therefore to reduce the power dissipation, MTCMOS technology by using the high Vt transistors S1(sleep NMOS) and S2(sleep PMOS) is used. Where S1 connects the virtual ground i.e node M in fig 7 to the actual ground, whereas the S2 connects the virtual supply i.e node N to the actual V_{dd} supply. This technique reduces both leakage power in sleep mode of the design as well the dynamic power. This design also has another low power technique used in it i.e charge recycling technique. This technique reduces static power dissipation during switching between active and sleep modes of the circuit. This technique is used by employing a transmission gate TG between the virtual ground (M) and the virtual supply (N). TG is turned on just before switching from sleep to active or active to sleep mode during write operation, to balance the leakage power thus reducing the static power of the design.

ADVANTAGE: This SRAM design has very less power and low power delay product (PDP) as compared to the 6T conventional SRAM design as well as with that of other discussed SRAM designs [10].

DISADVANTAGE: The design covers large area of the chip and has high access time as compared to the conventional 6T SRAM.

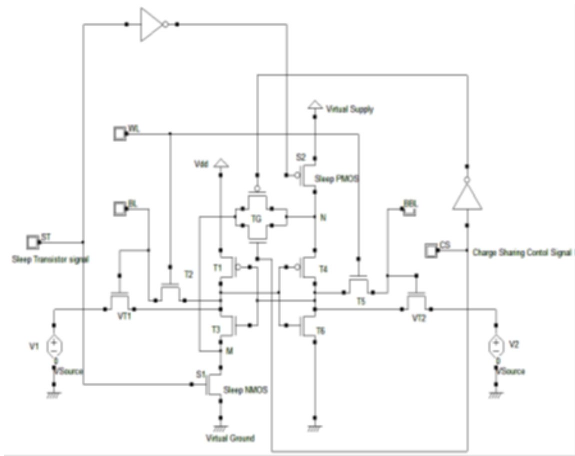

Figure 6 12T SRAM Design

Table 1 Comparison of power dissipation

Sram Designs	**Static power dissipation for write operation (µW)**	**Dynamic power dissipation for write operation (µW)**	**Static power dissipation for read operation (µW)**	**Dynamic power dissipation for read operation (µw)**
Conventional 6T SRAM[4]	6.263	9.234	7.731	6.967
Subthreshold 7T[6]	3.119	6.374	3.293	5.171
9T SRAM design[7]	6.117	7.901	5.992	7.901
PPN based differential 10T [8]	4.190	5.895	2.246	3.957
11T SRAM [9]	3.867	4.957	2.038	3.595
12T SRAM[10]	2.895	3.734	1.893	2.736

4.Conclusion

An extensive survey has been done for various Design of Static Random Access Memory. These designs are well preferred for various low power applications. Various techniques to reduce the power dissipation have been developed and it can be used for low power and high speed applications.

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