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Analysis of (SRAM) static random access memory power consumption

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Abstract

SRAM is a very critical component in several of the digital systems and electronic devices, from high-performance processors to mobile-phone chips. Power and system performance are the essential parameters for all applications. SRAM is small semiconductor memory cell. It is used one bit data for information storage in the form of electrical signal. It provides very fast speed operation and power consumption are very less as compared to other memory cells [1]. Portable electronic devices which are battery operated in which power consumption is major concern. The total power consumption in commercial processors and application specific integrated circuits increases with decreasing technology nodes. Total Power saving techniques in system has become a first class design point for current and future VLSI systems. Currently this technique is applied to study the power savings in application specific integrated circuit SRAM memories and can also be applied for commercial processors. By adding simple, low-overhead parity, an error-correction capability is added to the memory architecture for robust soft-error protection. Low power consumption in memory plays an important part in VLSI. But the memory consumes more power. The sub-threshold leakage power is the main reason for high power consumption.

Keywords

SRAM static RAM, Delay, speed, Power Consumption, Low Power, embedded dynamic-random-access-memory (eDRAMs).

1.Introduction

Total area and power consumption of the SOC devices, Occupied by static random access memory (SRAM), Increases largely with technology scaling . They are very critical components in both high-performance processors and hand-held device applications. The SRAM energy power becomes a major issue, and low power SRAM designs, without compromising any speed performance, are especially very crucial in modern very-large-scale integration (VLSI) designs. In order to improve the system's power efficiency, performance, reliability, and overall costs the attention has been need reduction of leakage current from SRAM cells,. The SRAM memory cell consumes energy in both dynamic and static ways. Historically, the primary source of total power dissipation has been dynamic energy due to word line decoding, bit line charging / discharging, sense amplification, and Output driving, and so on. In the system large Amount of data that needs to be handled by today's systems has increased the memory requirements, which already often occupy more than 50% of silicon real-estate and power in embedded systems. (eDRAMs) Dynamic-random-access-memory in embedded the popularity daily growing continuously because of their high level density and lower retention power features, in comparison of (SRAM) random access memory However, eDRAMs still require periodic, power-hungry refresh cycles to retain the stored data every time. Traditional design approaches dictate that the frequency of these refresh cycles is determined by the worst-case retention time of the most leaky cell. While such an approach guarantees error-free storage.

2.Review of related work

The (ITRS) International Technology Roadmap for Semiconductors predicts the gate equivalent oxide thickness as low as 0.5nm for upcoming future CMOS technologies [1]. Since the gate leakage current of MOS transistors increases continuously with the reduction of the oxide thickness over the active region of a transistor, the gate leakage power dissipation is expected to become very important factor in overall chip power dissipation in CMOS design processes [2]. The gate tunnelling current is predicted to increase at a rate of 500 times per technology generation where as the sub-threshold current increases by 5 times [1][3] with the dependency of leakage power on the number of transistors, also given the projected large memory content of future SoC (System on Chip) devices (more than 90% of the die area by 2014 [4]), it is most important to focus on minimizing the leakage power of SRAM cell structures.

There are several sources for the leakage current generation i.e. the sub-threshold current due to low threshold voltage, the gate leakage due to very thin gate oxides layer, and band-to-band tunnelling leakage due to heavily-doped doping profile structure [5]. Because of the exponential dependency of the gate leakage current on the oxide thickness, this current has the potential to become the dominant factor for future CMOS technologies.

The tunnelling current is composed of three major components:

(i) gate-to-source and gate-to-drain overlap currents (edge direct tunnelling current),

(ii) gate-to-channel current (direct tunnelling current), part of which goes to the source and the rest flows to the drain, and

(iii) gate-to substrate current [5].In higher level CMOS technology, the gate-to substrate leakage current is several orders of magnitude lower than the overlap tunnelling current and gate-to-channel current. In the ON state, in addition to the overlap tunnelling currents, the gate-to-channel tunnelling is added to the gate current increasing the total gate current. There are some techniques used for reducing the gate tunnelling leakage in digital circuits .These techniques reduces the leakage of the tunnelling currents on the terminal voltages.

The SOC devices consume total area and power consumption by (SRAM) static random access memory it Increase very largely with scaling in technology. Thus they are critical components in both high-performance processors and hand-held applications devices. Power consumption becomes a major issue continuously in SRAM, and low power SRAM designs, without compromising any speed performance are crucial in modern *very-large-scale integration* (VLSI) designing's. In fact, considerable attention has been contributed to the reduction of leakage current from SRAM cells, in order to improve the system's power efficiency, performance, reliability, and overall costs.

SRAM cell consumes power in both ways dynamic and static. Historically, the primary source of power dissipation has been dynamic energy due to word line decoding, bit line charging / discharging, sense amplification, output driving, and so on. If we directly move into sub-micron technology, the scaling of transistor threshold voltage sharply increases sub threshold leakage current supply power, whereas ultra-thin gate oxide results exponential increases gate leakage current. Figure 1 show the SRAM leakage current with technology scaling and it indicates that the leakage current has dramatically increased when technology scales down to 90 nm and below.

2.1Leakage current components

There are some sources of leakage current power supply, that is, the sub threshold current due to low threshold voltage, the gate leakage current due to very thin gate Oxides, and the band-to-band tunnelling current due to the heavily doped profile [1]

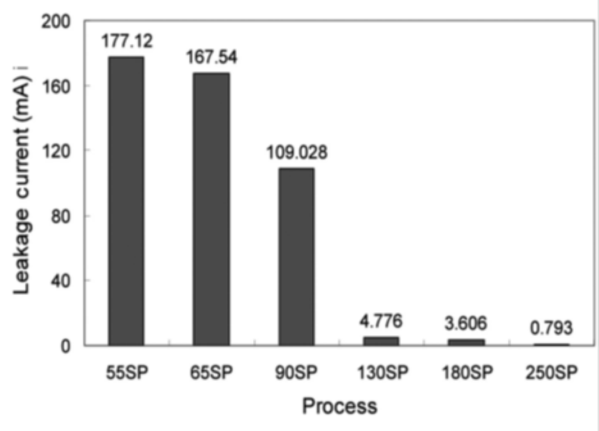

Figure 1 SRAM leakage current with technology scaling

(i) Sub threshold leakage current

This is part of leakage current the Sub threshold leakage current is the drain to source current of a transistor when supply of gate to source voltage is lower than the threshold voltage [2] and it is mainly composed of diffusion current. At present, the sub threshold leakage current still plays the main role in the three leakage mechanisms. There are two dominant sub threshold leakage paths in SRAM cell as shown in Figure 2: (1) V_{DD} to the ground and (2) bit lines to the ground, through access transistors. When the node nv0 stores '0', there is significant sub threshold leakage current through the off-transistors M1, M4, and access transistor M5, Whereas, that of M6 is negligible, because its source-drain voltage difference is zero.

(ii) Gate leakage current

If we reduce gate oxide thickness it results in an increase in the electric field across the oxide. Thus it leads to an exponential increase in tunnelling probability of electrons through the gate oxide, and it means an exponential increase in the gate oxide tunnelling current [17]. As the gate leakage current of the positive-channel metal–oxide–semiconductor (PMOS) transistor is about one order of magnitude smaller than that of negative channel metal–oxide–semiconductor (NMOS), the gate leakage current mainly flows through the NMOS transistors M4, M5, and M6, and the mechanism is primarily edge direct-tunnelling. Moreover, the gate leakage current of the on-transistor M3, that is primarily, direct tunnelling, is the maximum.

(iii) Junction leakage current

The reversed biased Positive-channel, Negative-channel (PN) junction leakage current has two main components: one corresponds to the minority carriers' diffusion near the edge of the depletion region, and the other is caused by an electron-hole pair generation in the depletion region of the reverse biased junction [2]. It is exponentially showing function of doping concentration and reverse biasing voltage across the junction. When we compared with other sources of leakage current, the junction current is quite small and mainly exists in access transistors M5 and M6, in a memory cell. Technology scaling, ultra-thin oxides and high doping concentrations have led to a rapid increase in gate leakage current and PN junction leakage current. The gate leakage current is even larger than the sub threshold leakage current from the 50 nm process downwards [15]. Consequently, all the three leakage current components used for standby leakage current reduction.

2.2 Leakage power reduction technologies

There are various types of techniques to deal with leakage power at different levels. In the device level, new material and process techniques have been introduced to control the channel length, oxide thickness, junction depth, and concentration distribution of transistors [3-5]. Novel transistor structures have been developed, for example, the Fin-Shaped Field Effect Transistor (FINFET), which has two or more gates to improve the gate control over the channel, leading to lower short channel effects and reduced sub threshold leakage current. There are many architectural level techniques such as multiple modes management have been presented, which put most unused memory sections into sleep or turn-off mode to achieve a large leakage current reduction [6,7]. Such a method is based on the fact that only a small fraction of SRAM works at a time.

(i) Body-biasing technique

The body-biasing technique is categorized as reverse body biasing and forward body-biasing. They are adopted to reduce the leakage current on the basis that the sub threshold leakage current is exponentially dependent on the threshold voltage. As Figure 4 show , the reverse body-biasing scheme is applied by raising or lowering VPWELL in standby mode condition, to produce body effect and thus to increase the threshold voltage [12-14]. Therefore, leakage sub threshold current decreases by increasing Vth. The active mode show body-biasing voltage is back to zero without affecting access time and data stability. The extra energy and time must be taken into consideration owing to the body-biasing mode transition operation. The effectiveness of the reverse body-biasing scheme decreases with technology scaling, due to worsening of the body effect caused by the shorter channel length. In addition, source-substrate, drain-substrate leakage current, and band-to-band tunnelling current exponentially increase at the source-substrate and drain-substrate PN junction.

A design can use the reverse body-biasing scheme in standby mode to reduce leakage current together with the forward body-biasing scheme in active mode for high performance, which is more effective than if only one of them is used in the design. Researchers have found that forward body-biasing and high V_{th} devices along with the reverse body-biasing scheme provide 20 times the leakage reduction, as opposed to three times the leakage reduction for the reverse body-biasing and low V_{th} devices [16].

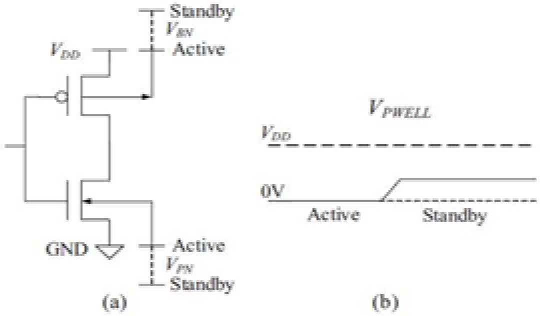

Figure 3 Body- biasing Technique

(ii) Source-biasing technique

In source biasing scheme we raises the ground voltage VSL in the standby mode [1, 17-21] to achieve a large reduction in the leakage current. Generally, a pull-down NMOS transistor M7 is inserted between the ground (GND) and source lines of the SRAM cell [17-20]. As shown in Figure 4, its gate terminal is connected to the word line (WL). In active mode, the WL goes high and then M7 is turned on. Its resistance is very small, the virtual ground voltage VSL almost functions as the real ground line and the SRAM cell works conventionally. In standby mode, WL is set low and M7 is turned off, thus raising the source voltage and reducing both the sub threshold and gate leakage current. The raised source voltage produces body effect, as the substrate voltage remains a constant. Hence, the threshold voltage increases, associated with the reduced signal rail

(VDD – VSL), and then the sub threshold leakage current is lowered. Same time, the gate leakage current also decreases due to the reduced potential of gate-source, gate-drain, and gate-substrate of most transistors in the SRAM cell. One drawback of this scheme is that the extra transistor M7 in the pull-down path will get a delay penalty, increasing both area and dynamic energy consumption. To minimize the area overhead, the pull-down transistor is often shared by a bank of SRAM cells. An IWL-VC SRAM has been proposed in Ref. [1],

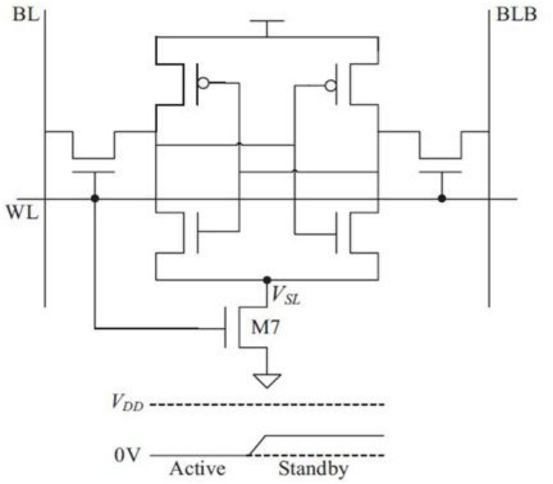

Figure 4 Source biasing Technique

which reduces the sub threshold leakage current by increasing the ground level during idle time with two NMOS transistors. Gate leakage current of access transistors is also lowered by the increasing word line voltage from VSS to Vth of the PMOS-controlled transistor.

(iii) Negative word line technique

The negative word line technique is used for generation of negative voltage supplied to the word line during idle Time [8-10] without affecting the device performance. In which the sub threshold leakage current of access transistors is reduced, as they are strongly turned off. At the same time, the gate leakage current of access transistors increases as a result of enlarged gate source and gate-drain voltage differences, as shown in Figure 5. Just like the dynamic *VDD* scheme, there is dynamic power overhead and an extra voltage generator needed for providing the negative voltage. A novel SRAM in which word line voltage is supplied with -0.2 V in standby mode, combined with a dynamic *VDD* scheme (0.2 V standby supply voltage) has been proposed [22-27].

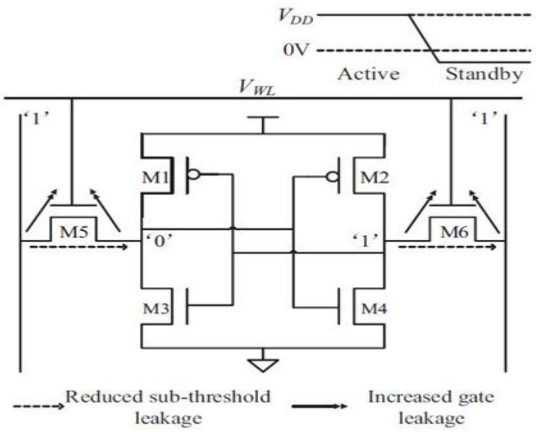

Figure 5 Negative word line technique

(iv) Sleep transistor technique

This technique is used to isolate the pull-up and pull-down networks from VDD and GND respectively. By using this isolation in sleep mode of operation the leakage power is reduced dramatically. But due to the extra circuitry area and delay of circuit are increased [6- 7].

(v) Forced stack technique

This technique uses a duplicate transistor for every transistor in network. Each transistor bears the half of the original transistor width. In the off state the duplicate transistor that produces a low reverse current supply from gate to source. Because of this reverse current power supply overall leakage current reduces SRAM using force stack technique

(vi) Sleepy stack technique

Sleepy stack technique is the combination of both techniques sleep transistor and forced stack method. This technique has lower leakage power dissipation, minimum delay and it also capable to retain the exact state. The sleep transistor of this technique works same as the sleep transistor technique. Sleep transistors are turned on during active mode and off in the sleep mode. This method achieves the faster switching than forced stack method.

3.Conclusion

Static Random Access Memory standby leakage power has become a major issue in modern low power SOC devices with technology scaling. In this paper we summarize the existing leakage reduction techniques, including body biasing, source biasing, sleep transistor schemes etc. We demonstrated that different techniques have different advantages and disadvantages. In a word, Sleep techniqur and source biasing schemes show greater leakage suppressing capability, whereas, the static noise margin of the other techniques almost keeps the same. As a result, the SRAM cell optimization must be seeking a tradeoffs Between power consumption and device performance.

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