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Clock gating techniques for the design of arithmetic and logic unit-a survey

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Abstract
This is often an era of devices which may be control in hands like cell phones, and private digital assistants. Since processors are often embedded in these devices this has became attainable. The 2 parameters that are important within the design of those systems are there in operation speeds and standby time. This paper presents a comparative study on different clock gating technique to cut back dynamic power consumption.

Keywords
Clock gating, Dynamic power consumption, FPGA.

1.Introduction
Portable devices with wireless network connections like Personal Digital Assistants (PDA), cellular phones and global Positioning System (GPS) navigators became increasing widespread and widely-used over the past few years. One reason for the widespread adoption is their usability like a change to a graphical interface. the flexibility for such a change has abundant to try to to with the high performance microprocessors embedded in them. Not solely are the microprocessors expected to execute difficult functions; however they additionally ought to sustain moderately long usage times giving rise to a desire for low power consumption. This explains why plenty of try and technological developments centre on building microprocessors that may deliver high performance and however consume nominal power. in this paper some techniques that are developed to scale back power consumption in microprocessors area unit mentioned. [14] [15].

Low Power processor Design is based on application of clock gate to turn off the sub-module of processor that is not in use by current executing instruction as decided by instruction decoder unit. According to [1]-[3], Clock Power consumes 50-70 percent of total chip power and will increase in the next coming generation of hardware designs at 32nm and below. Hence, reducing clock power is very important. Clock gating is a key power reduction technique used by hardware designers and is typically implemented by RTL-level HDL Simulator or gate level power analyzer tools.

$$Power = C_L \times (Voltage \times frequency) \quad (1)$$

In equation (1) power is directly proportional to the square of voltage and the frequency of the clock. Clock gating is used in VLSI circuit design to reduce dynamic power by gating off the functional unit that is not in use by current executing instructions as decided by instruction decoder unit.

The various clock gating techniques are listed below:
- Latch Free AND Clock Gating
- Clock Gating using NOR Gate
- Latch based AND Gate Clock Gating
- Latch based NOR Gate clock Gating
- MUX based Clock Gating
- Optimized Latch Based Clock Gating

Following sections will discuss above mentioned clock gating techniques.

2.Latch free AND clock gating
Initially many authors suggested using AND gate for Clock gating because of its simple logic [4][5][6]. In serial circuit one two-input logic gate is inserted in logic for clock gating. One input to logic gate is clock and whereas the second input could be a signal accustomed control the output (means it'll control the serial circuit's clock). For experimental purpose we tend to are taking an easy counter shown in Figure one as a serial circuit application. Figure two shows the wave of the output of standard counter, at first at reset = '0', counter initialized to "0" and afterward once reset='1' counter increments at every negative fringe of the clock. Figure three shows the clock gating technique for the counter by inserting one logic gate. Figure four shows the output of counter once counter is negative edge triggered and modify ('en') changes from clock cycle ranging from negative edge to consequent negative edge, during this case output of the counter changes when one clock cycle of being en='1'. From Figure five we've discovered that once counter is positive edge triggered and modify is dynamic ranging from positive edge to consequent positive edge, counter increments one time beyond regulation, thanks to little "Glitch", once it goes down due to additional falling time of

the modify, and also the output during this case is wrong. In Figure vi shows that for positive edge triggered system once modify activates at negative fringe of the clock to consequent negative edge, the counter increments just one time at positive fringe of the clock as a result of once modify goes down there's the negative fringe of the clock not positive. In Figure seven we've shown a significant drawback of Hazards once any hazard at the modify may be expire to the Gclk once clk='1' this example is especially very dangerous and might jeopardize the right functioning of the whole system [7][14] [15].

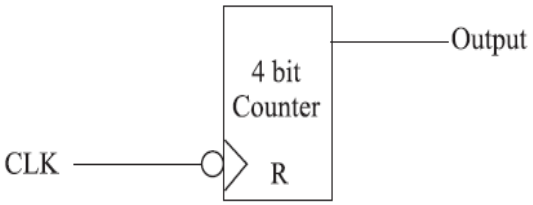

Figure 1 4 bit counter

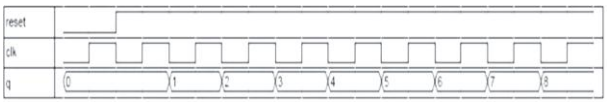

Figure 2 Normal output of counter without clock gating

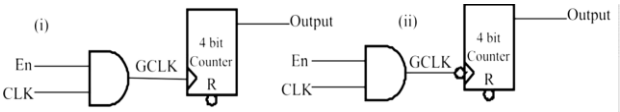

Figure 3 Clock gating using AND gate

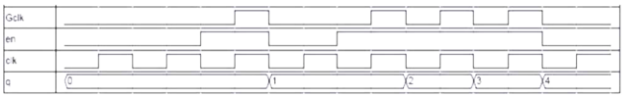

Figure 4 Output of counter when counter is negative edge triggered

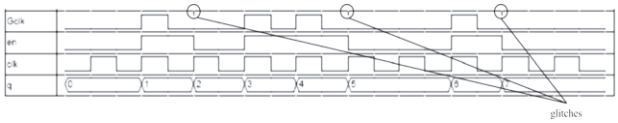

Figure 5 Wrong output of counter when it is positive edge triggered

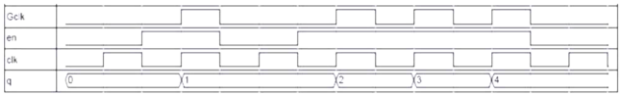

Figure 6 Correct output when counter is positive edge triggered

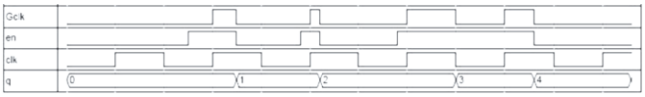

Figure 7 Hazard Problem when using AND gate clock gating technique

3.Clock Gating Using NOR gate

NOR gate is a very suitable technique for clock gating where we need actions to be performed on Positive Edge of the Global clock [7][6]. For analysis exploitation NOR gate, the circuit connection is shown in Figure 8; in this figure we are able to observe that Counter will work once modify flip "ON". Figure nine shows the undulation for incorrect output of the Counter once modify changes to '1' at negative fringe of the clock. Incorrect output is due to the little glitch once modify turns low at negative edge of the clock, counter increments one a lot of clock. Figure 10 shows output of Counter once modify changes from positive edge to next positive edge however counter is negative edge triggered. Figure eleven shows correct output of the counter with positive edge triggered as a result of modify is dynamic from positive fringe of the clock to succeeding positive fringe of the clock. within the figure twelve we've got shown a significant drawback of Hazards. once any hazard at the modify can be die to the Gclk once clk='0' this case is especially terribly dangerous and will jeopardize the proper functioning of the complete system [7][14][16].

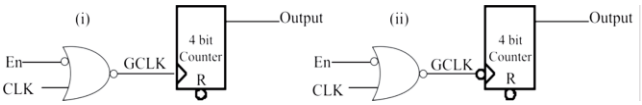

Figure 8: Clock gating using NOR gate

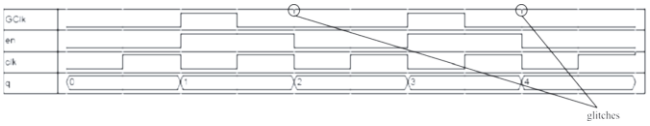

Figure 9: Incorrect Output of counter when counter is positive edge triggered

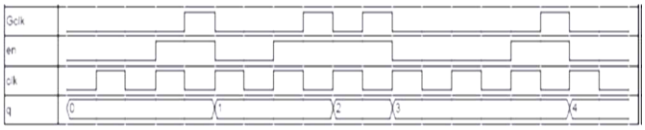

Figure 10 Output of Counter when enable changes from positive edge to next positive edge but counter is Negative edge Triggered

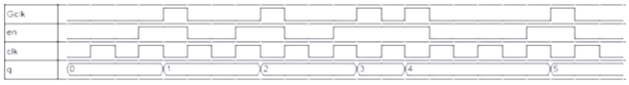

Figure 11 Correct output of Counter when Counter is positive edge triggered

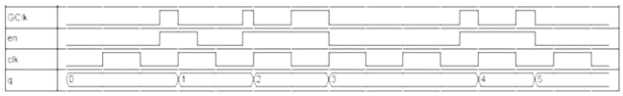

Figure 12 Hazards Problem when NOR Gate is used for clock gating

3.1Latch based AND Clock Gating

Latch based mostly AND Gated Clock circuit is shown in Figure 13. The enable signal 'En' is applied through a latch to beat the previous issues of incorrect output in place of directly connected to logic gate. The Latch is required for proper behavior, as a result of en might have Hazards that has got to not propagate through logic gate once global clock is '1' [9][12][8]. However, the delay of the logic for the computation of en could on the important path of the circuit can increase and its impact should be taken under consideration throughout time verification [12][10][8][11].

It is clear from Figure 14 that counter can take one additional clock cycle delay to vary its state and at that time it'll work commonly till, en is de-asserted and this point additionally it'll take one clock cycle additional to prevent dynamical its state. Figure 15 verifies that unwanted outputs as a result of Hazards at the nut ar avoided. Figure 17 wave form show that once dominant latch is positive and counter is additionally positive edge triggered then output of the counter is incorrect because it increments once even when enable is turned down due to a tiny glitch. [14][16].

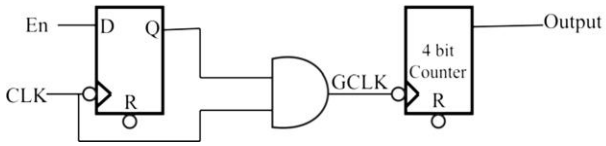

Figure 13 Flip Flop based clock gating technique

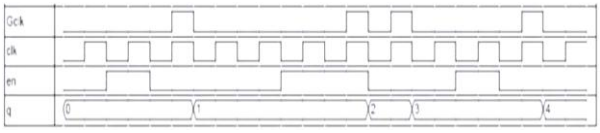

Figure 14 Normal output of negative edge counter when negative latch AND gated clock is used

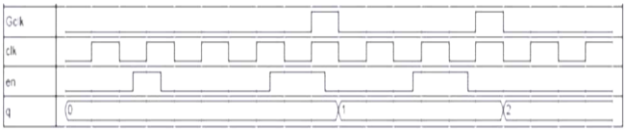

Figure 15 Output of negative edge counter when there is some random hazards at En

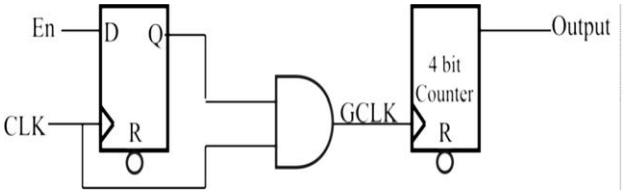

Figure 16 Clock gating of positive edge counter using positive latch Based and gate circuit

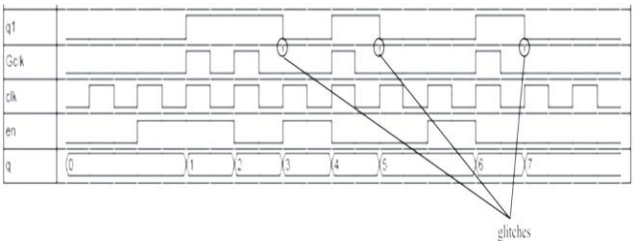

Figure 17 Output of counter when latch is positive and counter also positive edge triggered

4.Latch based NOR Gate clock Gating

Latch based NOR Gated Clock scheme is shown in Figure 18. Here enable signal is a applied through latch in place of direct connection to NOR gate. We can observe from Figure 19 that counter will take one extra clock cycle delay to change its state and after that it will work normally until En is de-asserted and this time also it will take one clock cycle extra to stop changing its state. In Figure 20 we have verified that unwanted outputs due to Glitches at the En are avoided. In Figure 22 waveform the case when controlling Latch is negative and Counter is also negative edge triggered is shown. The output of the counter is incorrect because it increments once even when enable is turned down due to a tiny glitch due to the fall time delay of enable.

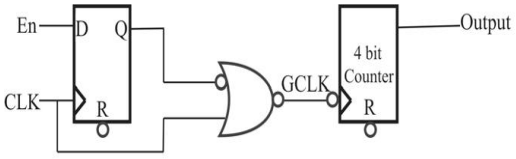

Figure 18 Clock gating of negative edge counter using positive latch based NOR gate circuit

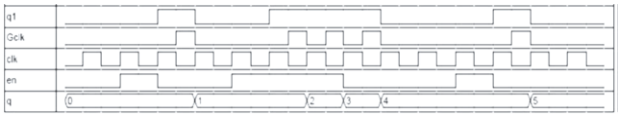

Figure 19 Normal output of negative edge counter when positive latch based OR Gated Clock is used

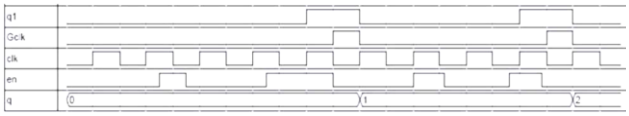

Figure 20 Output of negative edge counter when there are some random hazards at En

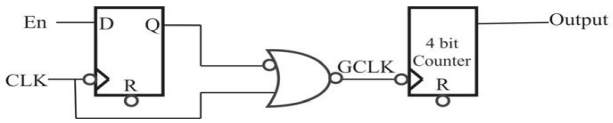

Figure 21 Clock gating of negative edge counter using negative latch based NOR gate circuit

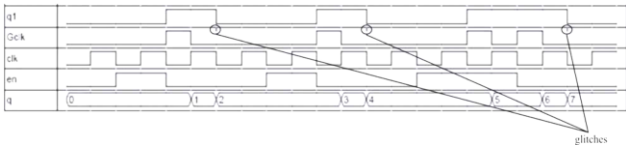

Figure 22 Output of counter when latch is negative and counter also negative edge triggered

5.MUX based Clock Gating

In mux based clock gating we use multiplexer to close and open a feedback loop around a basic D-type flip-flop under control of the enable signal as shown in Figure 23. As the resulting circuit is simple, robust, and compliant with the rules of synchronous design this is a safe and often also a reasonable choice. On the negative side, this approach takes one fairly expensive multiplexer per bit and consumes more power. This is because any toggling of the clock input of a disabled flip-flop amounts to wasting of energy in discharging and recharging the associated node capacitances for nothing. The capacitance of the CLK input is not the only contribution as any clock edge causes further nodes to toggle within the flip - flop itself [7]. In Figure 24 waveform of Negative Edge triggered Counter is shown and in 25 Positive edge triggered. We can observe from these waveforms that when En turns ON then at each Negative and Positive Edge of the clock respectively counter increments and when En goes Low counter holds its state.

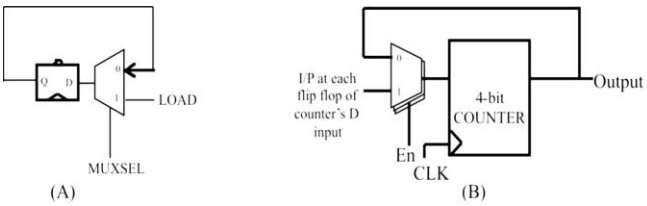

Figure 23 (A) Logic of MUX based Gated Clock (B) Counter using MUX based Clock Gating

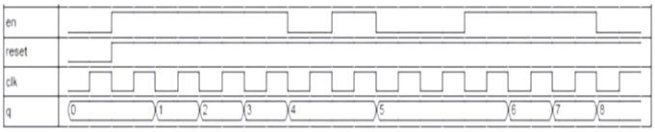

Figure 24 Output of negative edge triggered counter with MUX based clock Gating

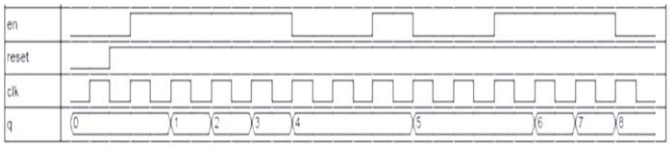

Figure 25 Output of positive edge triggered counter with MUX based clock Gating

6.Optimized latch based clock gating

An input signal named 'En' is provided to the latch. When En turns to '1' at that time GEN is '0', XNOR will produce x='0' which goes to the first clock generation logic that generates clock for controlling device (LATCH). In first logic we have an OR gate which have Global Clock as an input at the other input of OR gate. This logic will generate a clock pulse that will drive the controlling latch when 'x' turns to '0'.[7][14][15][16].

In the next clock pulse, when GEN turns to '1' our second clock generation logic which is an AND gate which has GEN and Global clk at its input and when Gen goes '1' it generates clock pulse that goes to the target device. Since GEN is '1' the XNOR will produce x='1' thus OR will produce at CClk constant HIGH until En turns to '0'. This way GClk will be running and CClk will be at Constant '1' state that means latch will hold its state without any switching.
The circuit shown in figure 27 performs similar sequence of operations as explained for the circuit shown in Figure 26. When En turns to '1' at that time GEN is '0' so XOR will produce x='1' which matches to the primary clock generation logic that generates clock for dominant device (LATCH). In initial logic we've got an logic gate, that have global Clock as an input at the opposite input of logic gate. This logic can generate a clock pulse that can drive the dominant latch once 'x' turns to '1'. within the next

clock pulse, once info turns to '1' our second clock generation logic that is associate gate that has q and global clock at its input and once q goes '0' it generates clock pulse that goes to the target device. Since gen is '1' the XOR will turn out x='0' therefore OR can turn out at CClk constant LOW till linear unit turns to '0'. this manner GClk are going to be running and CClk are going to be at Constant '0' state which means latch can hold its state with none change. [7][15].

The output of Counter for circuit as in Figure 26 is shown in Figure 28, 29. In Figures 28 and 29 modify changes from negative edge to next negative edge and positive edge to next positive edge respectively and also target is negative edge triggered and positive edge triggered respectively. However, in each cases counter's state dynamic delay is totally different however output is correct which provides us answer of the matter that persists in initial four kinds of clock gating.[14][15][16].

The output of Counter for circuit as in Figure 27 is shown in Figure 30 & 31. In figure 30 & 31 enable changes from negative edge to next negative edge and positive edge to next positive edge respectively and also target is negative edge triggered and positive edge triggered respectively. However, in both cases counter's state changing delay is different but output is correct which gives us solution of the problem that persists in first four types of clock gating. Thus one can avoid more switching and can save power.

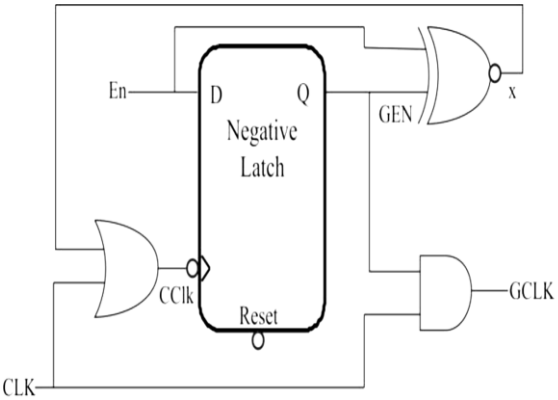

Figure 26 Generation of gated clock when negative latch is used

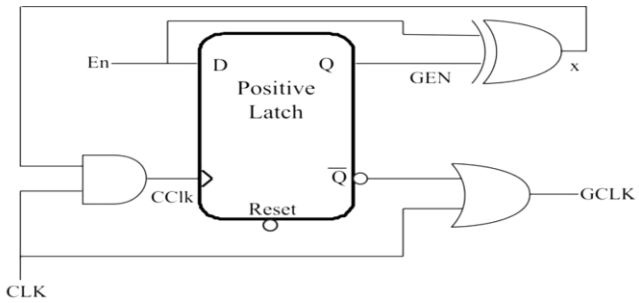

Figure 27 Generation of gated clock when positive Latch is used

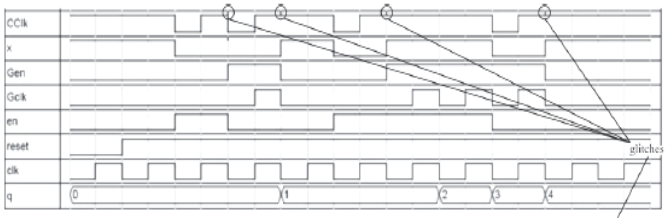

Figure 28 Output of negative edge counter with gated clock for circuit 26

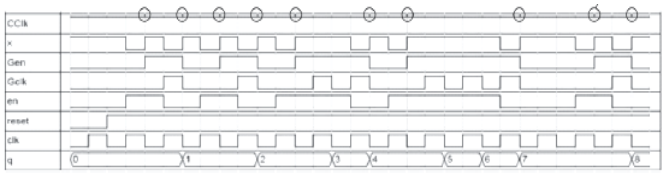

Figure 29 Output of positive edge counter with gated clock for circuit 26

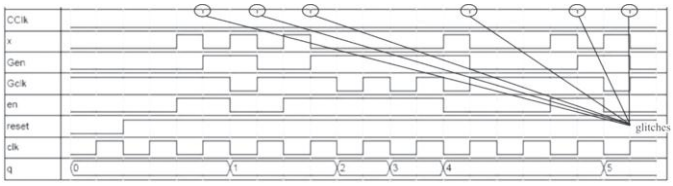

Figure 30 Output of negative edge counter with gated clock for circuit 27

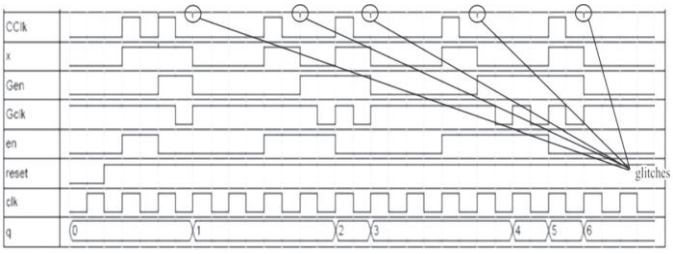

Figure 31 Output of positive edge counter with gated clock for circuit 27

7.Conclusion

This paper we have reviewed different clock gating techniques. Hazard is the basic problem associated with all the clock gating techniques discussed in section II to V. in section VI mux based clock gating technique is discussed which didn't have this problem. In the end a optimized clock gating scheme is discussed, this technique is hazard free and also reduces the power consumption more effectively compared to other methods discussed.

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