Survey of low power and area efficient XOR/XNOR gate using CMOS logic design

Kirti Dhakad[1] and Shraddha Shrivastava[2]
M. Tech Scholar, LNCT, Bhopal[1]
Assistant Professor, LNCT, Bhopal[2]

Abstract

The quick developments of compact electronic gadgets are expanded and they are planning with low power and rapid is basic. To plan a three info XOR and XNOR entryways utilizing the methodical cell outline philosophy can be accomplished by actualizing transmission door. By this kind of planning the low power and fast can accomplished. This engineering is utilized to keep up summation comes about for subsequent to finishing expansion process.

Keywords

Reversible gates, Reversible encoder, Reversible decoder.

1.Introduction

The quick development of convenient electronic gadgets is a basic test to configuration low-control, rapid circuits that involve little chip territories. Such examinations for the most part depend on inventive plan musings yet don't take after a methodical approach. As significance, a large portion of them experience the ill effects of some extraordinary downside. 1. They are executed with rationale styles that have an inadequate voltage swing in some inner hubs, which prompts the static power dispersal. 2. The majority of them experience from extreme yield flag debasement and can't manage low voltage task. 3. They dominatingly have dynamic power utilization for non-adjusted proliferation delay inside and outside circuits, which brings about glitches at the yields. An efficient outline technique can be viewed as a solid elucidation for the test. It is not try and-error-driven, which means that it systematically and intentionally aims to design goals. It also picks circuit components wisely and does not postpone the determination of the circuit characteristics after simulation. Cell design methodology (CDM) has been presented to design some narrow functions, such as two input XOR/XNOR and carry–inverse carry in the hybrid-CMOS style. The predominant results persuade us to develop CDM through two stages: 1. Generating more complex functions and 2. Rectifying some remaining flaws. The exclusive-OR (XOR) and exclusive-NOR (XNOR) gate is the critical parts of several digital systems and it is highly used for very large scale integration (VLSI) system. The XOR/XNOR circuits used in parity checkers, comparators, crypto processors, arithmetic and logic circuits, test pattern generators. The SCDM methodology for design a XOR/XNORs gate and design is implemented. The first time Systematic Cell Design Methodology (SCDM) designing a three-input XOR/XNORs. Its systematically generates elementary basic cell (EBC) by using the binary decision diagram (BDD), and wisely chooses circuit components based on a specific target. Therefore, after the systematic generation, the SCDM considers circuit optimization based on our objective in three steps: 1. Wise selection of the basic cell; 2. Wise selection of the amend mechanisms; 3. Transistor sizing. The motivation to use this methodology is the presence of some unique features and the capability to produce some effective circuits that enjoy all these benefits. 1. The methodology has high flexibility in goal and systematically considers it in the three design steps. This can lead to effective circuits in terms of performance, power, Power Delay Product (PDP), Energy Delay Product (EDP), area, or a combination of them.

Efficient Cell Design Methodology (SCDM) builds up the guides of various rationale styles as the half and half style. 3. Minimal number of transistors in basic way expands the odds of the circuit to have better qualities. 4. The dynamic utilization enhancement originates from the reality of all around adjusted proliferation delay. 5. Symmetrical structure, high measured quality, and general plan of outlines offer increment to sharing more wells of associated transistors and thus decreasing the possessed region. 6. The debasement in all yield voltage swing would thus be able to be at last expelled, which makes the plan economical in low Vdd activities and low static power dispersal. 7. Inner rationale structure of plans can possibly be vitality effective and because of the joined diminishment of energy utilization and proliferation delay.

2.PENTA-MTJ

Passage magnetoresistance (TMR) is a magneto resistive impact that happens in an attractive passage intersection (MTJ), which is a segment comprising of two ferrimagnets isolated by a thin separator. On the off chance that the protecting layer is sufficiently thin regularly a couple of nanometers, electrons can burrow from one ferrimagnet into the other. Since this procedure is illegal in established material science, the passage magnetoresistance is an entirely quantum mechanical marvel. Attractive passage intersections are produced in thin film innovation. On a mechanical scale the film testimony is finished by magnetron sputter statement; on a research facility scale atomic pillar epitaxy, beat laser affidavit and electron shaft physical vapor testimony are additionally used. The intersections are set up by photolithography.

Combinational Circuits

Combinational circuit is a circuit in which we combine the different gates in the circuit, for example encoder decoder, multiplexer and de multiplexer. Some of the characteristics of combinational circuits are following –

1) The output of combinational circuit at any instant of time depends only on the levels present at input terminals.
2) The combinational circuit do not use any memory. The previous state of input does not have any effect on the present state of the circuit.
3) A combinational circuit can have an n number of inputs and m number of outputs

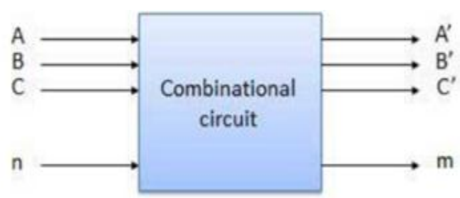

Figure 1 Block diagram of combinational circuit

Sequential Circuits:-

There are two types of input to the combinational logic; External inputs which come from outside the circuit design and are not controlled by the circuit; Internal inputs which a function of a previous output states are. The internal inputs and outputs are referred to as "secondaries" in the course notes.

The combinational circuit does not use any memory. Hence the previous state of input does not have any effect on the present state of the circuit. But sequential circuit has memory so output can vary based on input. This type of circuits uses previous input, output, clock and a memory element.

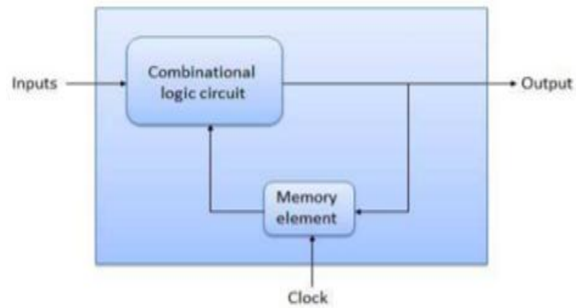

Figure 2 block diagram of sequential circuit

3.Literature review

Mohit Kumar Gupta et al. [1], advanced computing systems embed spintronic devices to improve the leakage performance of conventional CMOS systems. High speed, low power, and infinite endurance are important properties of magnetic tunnel junction (MTJ), a spintronic device, which assures its use in memories and logic circuits. This paper presents a Penta MTJ-based logic gate, which provides easy cascading, self-referencing, less voltage headroom problem in precharge sense amplifier and low area overhead contrary to existing MTJ-based gates. Penta MTJ is used here because it provides guaranteed disturbance free reading and increased tolerance to process variations along with compatibility with CMOS process. The logic gate is validated by simulation at the 45-nm technology node using a Verilog A model of the Penta MTJ.

S. D. Pable et al. [2], designing ultralow-power (ULP) efficient very large scale integration digital circuits have received widespread attention due to the rapid growth of portable applications. Device operating in subthreshold region has a strong potential toward satisfying the ULP conditions of portable systems. This paper mainly investigated and compared the performance of single-wall carbon nanotube (SWCNT), Cu, and mixed CNT bundle interconnects for different interconnect lengths and biasing levels under subthreshold conditions. It proposes that individual SWCNT can be used for short and intermediate length interconnects at different bias points in the subthreshold region due to less critical interconnect resistance contrary to super threshold region. Furthermore, performance analysis of global interconnect shows that in moderate subthreshold region, scaled Cu interconnect performs better than individual SWCNT and mixed CNT bundle, whereas in deep subthreshold region individual SWCNT is still better.

H.-P. Trinh et al. [3], the miniaturization of integrated circuits based on complementary metal oxide semiconductor (CMOS) technology meets a significant slowdown in this decade due to several technological and scientific difficulties. Spintronic devices such as magnetic tunnel junction (MTJ) nanopillar become one of the most promising candidates for the next generation of memory and logic chips thanks to their non-volatility, infinite endurance, and high density. A magnetic processor based on spintronic devices is then expected to overcome the issue of increasing standby power due to leakage currents and high dynamic power dedicated to data moving. For the purpose of fabricating such a non-volatile magnetic processor, a new design of multi-bit magnetic adder (MA)-the basic element of arithmetic/logic unit for any processor-whose input and output data are stored in perpendicular magnetic anisotropy (PMA) domain wall (DW) racetrack memory (RM)-is presented in this paper. The proposed multi-bit MA circuit promises nearly zero standby power, instant ON/OFF capability, and smaller die area. By using an accurate racetrack memory spice model, we validated this design and simulated its performance such as speed, power and area, etc.

S. Lee et al. [4], a magnetic-tunnel-junction (MTJ) element have been widely studied for data storage applications. An MTJ element can also be used to compute Boolean functions and store the output result. A magneto logic device based on this MTJ element can constitute sequential logic functions as well as combinational logic. Counter is one of the most frequently used sequential logic blocks in digital logic systems. In this paper, a novel architecture of a 3-bit gray counter based on magneto logic elements is presented. It is shown that ten MTJ elements with complementary metal-oxide-semiconductor (CMOS) circuits for sense amplifier and writing-current driver can make a 3-bit gray counter. HSPICE simulation results are presented to verify the functionality of the proposed circuits.

Lyle et al. [5], we investigated magnetic tunnel junction (MTJ)-based circuit that allows direct communication between elements without intermediate sensing amplifiers. Two- and three-input circuits that consist of two and three MTJs connected in parallel, respectively, were fabricated and are compared. The direct communication is realized by connecting the output in series with the input and applying voltage across the series connections. The logic circuit relies on the fact that a change in resistance at the input modulates the voltage that is needed to supply the critical current for spin-transfer torque switching the output. The change in the resistance at the input resulted in a voltage swing of 50-200 mV and 250-300 mV for the closest input states for the three and two input designs, respectively. The two input logic gate realizes the AND, NAND, NOR, and OR logic functions. The three-input logic function realizes the majority, AND, NAND, NOR, and OR logic operations.

4.Methodology

In order to generate the EBC of three-input XOR/XNOR circuits, four steps are taken. Initially, three-input XOR and its complement are represented by one binary decision tree (BDT) in order to share common sub circuits. The BDT is achieved by some cascaded 2 ×1 MUX blocks, which are denoted by simplified symbol controlled with input variables at each correspondent level. This construction simply implements the min-terms of the three-input XOR/XNOR function. The step is followed by applying reduction rules to simplify the BDT representation. These include elimination, merging, and coupling rules. The major task of the coupling rule, in simple terms, is to obtain all the possible equivalent trees by interchanging the order of the controls. The trees are acquired by impacting the state matrix on the corresponding control matrix where the multiply and add operators operate as follows. The result of applying the reduction rules to the tree. Afterward, as the inputs into the first level are 0's and 1's of the function's truth table, the 0 and 1 can be replaced by the Y' and Y , respectively. Finally, the simplified symbol can be divided into two distinct symbols: 1) the plus sign with the x input control and 2) the minus sign with the x_ input control. The result of applying steps 3 and 4. The EBC, which is extracted from the above procedure, has been presented[6-8]. This cell has eight elements, deciding two outputs. We refer to the pins of the central section (IN1–IN4 and G1–G4) as A or C, or their complements. We also assume that pins of the external section G5–G8 can also be B or its complement.

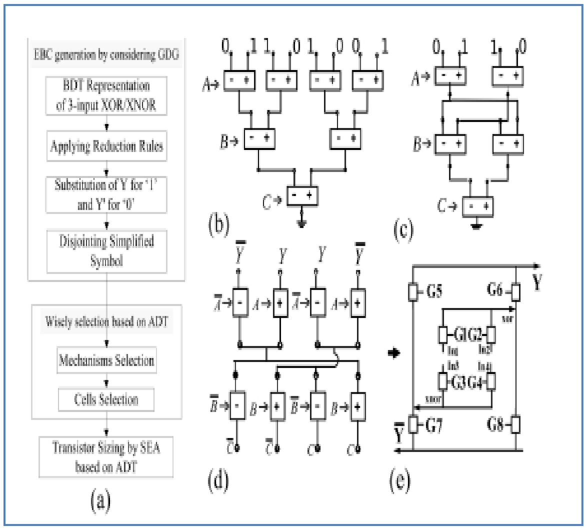

Figure 3 SCDM Process for Designing Efficient Three-Input XOR/XNOR. (b) BDT Representation of Three-Input XOR/XNOR Function. (c) Applying Reduction Rules. (d) Substitution and Disjointing. (e) EBC [2]

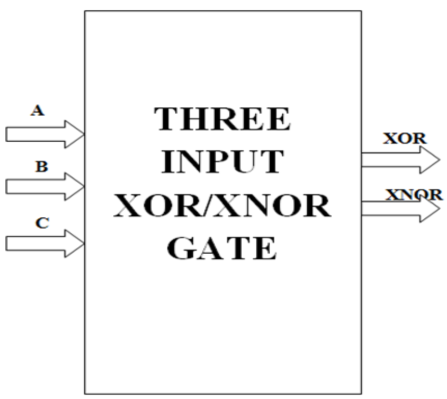

Figure 4 Block Diagram of Simple Three Input XOR/XNOR Gate

A block diagram is in Figure 4. Normally, we know that, three input xor/xonor operates the binary no. and accounts for values carried in as well as out. A three input xor /xnor operates three one-bit numbers, often written as A, B, and C.

5.Simulation tool

Environment setup is the work environment or tools on which result analysis has been done for Xilinx 6.2i. Xilinx is the very strong software tool to analysis and simulate the complex circuits. There are so many versions for Xilinx software such as 6.1i, 9.1i, 10.2i, 13.1i and 14.2i. Generally two programming language are using VHDL and Verilog. VHDL is an acronym for VHSIC hardware description language (VHSIC is an acronym for very high speed integrated circuits). It is a hardware description language that can be used to model a digital system at many levels of absorption ranging from the algorithm level to the gate level [9-16]. VHDL allows users or programmers to use certain blocks which comprise of certain set of sequential statements. One such block is called a process. The (<=) operator, it is called the assignment operator and is used only for assigning values to signals. For variables the operator used is (:=).

Some chief terms that are used at the basic level are: - Libraries, Data types, Signals, Variables, Entity, and Architecture. Other important terms for the VHDL program such as process, component, function, procedures and state diagrams are used in programming.

6.Conclusion

In nanometre scale CMOS technology, sub threshold leakage power is compatible to dynamic power consumption, and thus handling leakage power is a great challenge. In this dissertation, a new circuit design named “Low Power and area efficient of Three Input XOR/XNOR Gate Using CMOS Logic Design” to tackle the leakage problem will be discussed.

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