Review of reversible encoder and decoder using reversible gate

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Abstract

In today's world reversible encoder and decoder is one of the very important parts of any system having many applications in computers, mobile, calculators etc. Reversible logic is useful in mechanical applications of nanotechnology, given that the friction generated by contacting corpuscles within a confined volume can be significantly reduced by eliminating sliding contact using mechanical reversible logic. We have implemented reversible arithmetic logic unit based on reversible encoder and decoder. The problem of minimizing the number of garbage outputs is an important issue in reversible logic design. Reversible encoder and decoder are consisting of different gate.

Keywords

Reversible gates, Reversible encoder, Reversible decoder.

1.Introduction

Most conventional PCs lose data during the time spent calculation. Consider the straightforward two information Boolean AND entryway: Observing a yield of 0 does not give enough data to recognize the information mix that offered ascend to the yield. Truth be told, any of three distinctive information mixes (00, 01, 10) would constrain the yield of the AND entryway to 0. In registering the consistent AND of two bits, a conventional AND door would dispose of that info data. The main characteristically consistently reversible conventional natives incorporate the wire and inverter. The finishes of Landauer and Bennett demonstrate that a vitality loss of kTln2 joules as warmth unavoidably goes with each piece of data disposed of amid calculation, and that a totally reversible PC is hypothetically conceivable [1, 2]. Just by playing out the calculation in a sensibly reversible way would energy be able to scattering fall underneath kTln2 joules per bit per cycle.

Power crisis is a vital problem in today's world. In recent years, the growing market of electronic systems suffers from power dissipation and heat removal problem. If more and more power is dissipated, system becomes over heated which reduces the life time of the electronic system. The need of microelectronic circuits with low power dissipation leads to the implementation of reversible logic circuit. Bennett [3] proved that the one-to-one mapping between the inputs and outputs of reversible circuit drastically reduces the power consumption and heat dissipation of a circuit. Today security in digital computing and communications is of prime importance and therefore cryptographic protocols play a major role.

There are four major design parameters of reversible circuits. First is the quantum cost which is the number of basic quantum gates like Controlled NOT, Controlled V+ etc. in the reversible circuit. Second is the quantum depth also called quantum delay [4]. Third is the number of ancillary inputs or ancilla inputs which are constant inputs which are used to maintain the reversibility of the device. Fourth is the number of garbage outputs i.e. output signals which are not used as inputs to other gates and are only there to maintain reversibility.

2.Reversible Gate

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is the only 2x2 reversible gate available. It is most commonly used for fan out purposes. The 3x3 reversible gates include Toffoli gate, Fredkin gate, new gate and Peres gate, all of which can be used to realize the various Boolean functions in various logical architectures.

Basic Reversible Gates

Several reversible logic gates are used in previous design. In figure 1, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

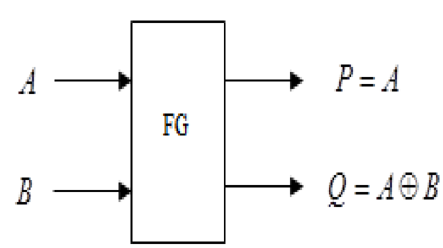

Figure 1 Feynman gate

In Figure 2, the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

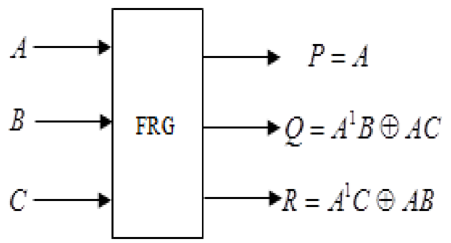

Figure 2 Fredkin gate

Figure 3 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstanding the fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

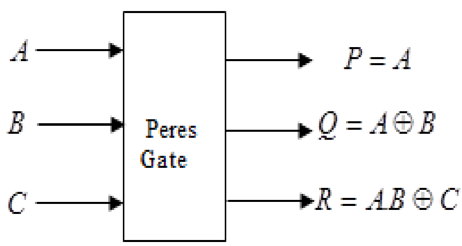

Figure 3 Peres gate

The HNG gate, presented in fig, produces the following logical output calculations:

$$P = A \quad (1)$$

$$Q = B \quad (2)$$

$$R = A \oplus B \oplus C \quad (3)$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \quad (4)$$

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Figure 4.

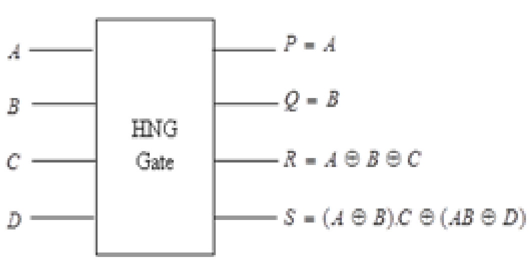

Figure 4 Block Diagram of the HNG Gate

A new programmable 4x4 reversible logic structure - Peres And-Or (PAOG) gate – is presented which produces outputs

$$P = A \quad (5)$$

$$Q = A \oplus B \quad (6)$$

$$R = AB \oplus C \quad (7)$$

$$S = (AB \oplus C).C \oplus ((A \oplus B) \oplus D) \quad (8)$$

Figure 5 shows the block diagram of the PAOG gate. This gate is an extension of the Peres gate for ALU realization.

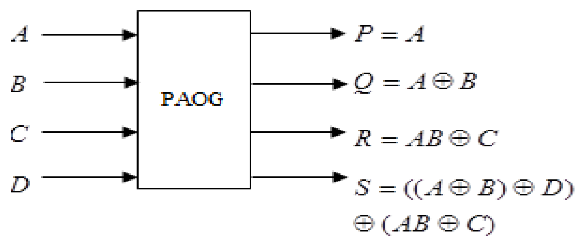

Figure 5 Block Diagram of the PAOG

Several 4x4 gates have been described in the literature targeting low cost and delay which may be implemented in a programmable manner to produce a high number of logical calculations. The DKG gate produces the following logical output calculations:

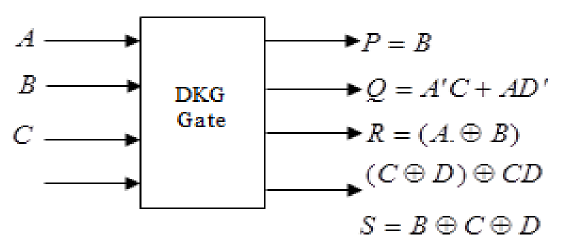

Figure 6 DKG Gate

$$P = B \quad (9)$$

$$Q = A'C + AD' \quad (10)$$

$$R = (A \oplus B)(C \oplus D) \oplus CD \quad (11)$$

$$S = B \oplus C \oplus D \quad (12)$$

3.Literature review

Gopi Chand Naguboina et al. (2017, [1]), reversible rationale is the rising field for inquire about in display period. The point of this paper is to acknowledge distinctive sorts of combinational circuits like full-snake, full-subtractor, multiplexer and comparator utilizing reversible decoder circuit with least quantum cost. Reversible decoder is planned utilizing Fredkin doors with least Quantum cost. There are numerous reversible rationale doors like Fredkin Gate, Feynman Gate, Double Feynman Gate, Peres Gate, Seynman Gate and some more. Reversible rationale is characterized as the rationale in which the number yield lines are equivalent to the quantity of information lines i.e., the n-info and k-yield Boolean capacity F(X1, X2, X3,… ,Xn) (alluded to as (n, k) work) is said to be reversible if and just on the off chance that (I) n is equivalent to k and (ii) each information design is mapped particularly to yield design. The entryway must keep running forward and in reverse that is the information sources can likewise be recovered from yields. At the point when the gadget complies with these two conditions then the second law of thermo-flow ensures that it disseminates no warmth. Fan-out and Feed-back are not permitted in Logical Reversibility. Reversible Logic possesses its applications in different fields which incorporate Quantum Computing, Optical Computing, Nanotechnology, Computer Graphics, low power VLSI Etc., Reversible rationale is picking up its own particular significance lately to a great extent because of its property of low power utilization. The near investigation regarding refuse yields, Quantum Cost, quantities of doors are likewise introduced. The Circuit has been actualized and reproduced utilizing Xilinx programming.

Michael Nachigal et al. (2016, [2]), the design of encoder/decoder can be analyzed in terms of quantum cost, garbage outputs, constant inputs. Reversible computational work totally differs from traditional computation, as it preserves information while manipulating it. Various reversible combinational and sequential designs have been implemented based on reversibility nature of the circuit. Very little focus has been done on reversible encoder/decoder design. The author proposed a novel design, where 2:4 encoder and decoder are implemented by using Friedkin gates whose quantum cost associated is 5 instead of peres gate whose quantum cost is 4. This work also represents the improvement in garbage output that is added to a multiple output function to make it reversible. Implemented or proposed design for decoder/encoder improves over existing design in terms of performance metrics except for the delay.

Md. Shamsujjoha et al. (2015, [3]), by stating that a fault tolerance gate (F2G) itself work as 2 to 1 reversible decoder. A fault tolerance reversible decoder has its application in Multiple-symbol differential detection, parallel circuits, network components etc. One F2G and two FRG are used to realize 2 to 4 fault tolerance reversible decoder. Further design can be extended to 3 to 8 reversible decoder using FRG gates and Feynman double gate. Similarly a reversible 4 to 2 encoder design which behaves like a traditional encoder i.e., exactly one of its four inputs will have the value of logical 1 at any point. The design has zero constant inputs and two garbage outputs. Constructed circuits can detect any type of single bit error for stuck-at fault. This technique also minimizes the garbage outputs during the process of conversion to testable, but the design is not much optimized in terms of quantum gates, constant input, and delay.

Nusrat Jahan Lisa et al. (2014, [4]), outlines a 2 to 4 decoder, which produces every one of the four essential AND capacities utilizing 1 Peres door and 3 CNOT entryway, in this way an aggregate number of quantum doors are seven. The plan can be reached out to 3 to 8 decoder utilizing 2 to 4 decoder circuit and four Fredkin doors and 4 to 16 decoder circuit utilizing three 2 to 4 decoder and eight fredkin entryways. Additionally, speak to the properties of n to the 2n reversible decoder with a summed up calculation. Configuration significantly enhances over a traditional outline of decoder can be developed to enhance the waste yield comes at the cost of a somewhat higher quantum cost. Arvind Kumar et al. [9] inferred that the 2 to 4 decoder utilizes fredkin entryways. Since every one of the three fredkin entryways are reversible in nature consequently having less power dissemination. Configuration can be reached out up to n to 2n decoder. A 4 to 16 decoder has been outlined utilizations 15 consistent sources of info and 4 junk yields. This work is very viable as far as execution with three fredkin entryway; add up to defer will be more which thus prompts more power dissemination guarantees that this plan isn't a compelling methodology.

4.Simulation tool

Environment setup is the work environment or tools on which result analysis has been done for Xilinx 6.2i. Xilinx is the very strong software tool to analysis and simulate the complex circuits. There are

so many versions for Xilinx software such as 6.1i, 9.1i, 10.2i, 13.1i and 14.2i. Generally two programming language are using VHDL and Verilog. VHDL is an acronym for VHSIC hardware description language (VHSIC is an acronym for very high speed integrated circuits). It is a hardware description language that can be used to model a digital system at many levels of absorption ranging from the algorithm level to the gate level [14]. VHDL allows users or programmers to use certain blocks which comprise of certain set of sequential statements. One such block is called a process. The (<=) operator, it is called the assignment operator and is used only for assigning values to signals. For variables the operator used is (:=).
Some chief terms that are used at the basic level are: - Libraries, Data types, Signals, Variables, Entity, and Architecture. Other important terms for the VHDL program such as process, component, function, procedures and state diagrams are used in programming.

Reversible Gate Parameter:-
Gate Count (GC): The number of gates used to realize reversible circuit
Garbage Outputs (GO): The number of unused outputs in a reversible logic. The inputs regenerated at the outputs are not garbage outputs.
Ancilla Inputs (AI): The number of input kept constant at either 0 or 1.
Delay : It corresponds to number of primitive quantum gates in the critical path of the circuit.
Quantum Cost:- Quantum cost is defined, as the number of basic quantum gates like controlled-NOT, Controlled V+, Controlled V and NOT gate.

5.Expected outcomes

The resulting VHDL simulation models can then be used as building blocks in larger circuits (using schematics, block diagrams, or system-level VHDL descriptions) for the purpose of simulation.

1. Design 64-bit, 32-bit, 16-bit, 8-bit, 4-bit and 2-bit encoder and decoder using different types of reversible gate.
2. Design different types of programmable reversible gate and compared.
3. Design free garbage based architecture using different types of input and compared existing algorithm.
4. Hand calculation of delay and area in reversible arithmetic logic unit in different inputs.
5. All the modules design to different device family i.e. Spartan-3, Virtex-4 and Virtex-7.

6.Conclusion

This thesis mainly focuses on a novel design of reversible processor components. Internal architecture components I;e, ALU, CU, register files and PC having better performance with proposed circuitry as compared to previous counterparts. Also, registers and the memory for program and data fall into the category of improved performance with reduced delay. Memory access pattern, execution, and complexity of instruction are kept in mind improve the execution time by using Harvard architecture instead of von Neumann. Power dissipation is also less about negligible since an overall system is designed using reversible nature of logics. With all above demonstration, using proposed designs improve the performance of CPU and execution time will be faster.

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