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DESIGN METHODOLOGY OF NUMERICALLY CONTROLLED OSCILLATOR FOR DIGITAL WAVEFORM GENERATION

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Abstract
Numerically Controlled Oscillator (NCO) is the fundamental block for digital waveform generation currently being widely used in aerospace, mobile communication, satellite communication, navigation systems and radars. The design and implementation methodology of NCO is very crucial to meet the targeted specification of precise frequency control, phase control etc. along with additional constraints of low power, small area and lesser implementation/design time. This paper addresses design methodology of NCO meeting all these constraints for two important applications, Direct Digital Frequency Synthesizer (DDFS) and Digital up Converter (DUC)/ Digital down Converter (DDC).

Keywords
NCO, DDFS, DUC/DDC, FPGA, High Speed DAC, High Speed ADC

1.Introduction
Numerically Controlled Oscillator is a digital signal generator which generates a discrete-time, discrete-value form of any waveform like pulse, triangle, and sinusoidal signal. Digital means of waveform generation was proposed by Tierney in 1971 known as Direct Digital Synthesis [1] (DDS) or Direct Digital Frequency Synthesis (DDFS), which is a mixed signal system consisting of digital system and analog system. Numerically controlled oscillator (NCO) is the digital part which takes samples of signal waveform at very small phase interval, their amplitudes corresponding to phases were stored in ROM (Read Only memory). This method offer advantages such as precise frequency & phase resolution, short conversion time, high reliability, easy debugging & easy integration[2]-[5], over other conventional methods such as direct analog frequency synthesis and indirect frequency synthesis[6]-[11]. Direct analog frequency sysnthesis method employs mathematical operation such as addition, subtraction, multiplication, division on various analog reference source. Implementation of these operations via analog methods makes overall system bulky and power hungry. Indirect frequency synthesis employs phase feedback and phase locked technology, phase locked loop (PLL) along with Voltage Controlled Oscillator (VCO) to generate signals, this methods produces high output frequency signal however due to closed loop control their circuit implementation is complex, difficult to debug. Due to various advantages offered by DDFS its application in the fields of mobile communication, satellite communication, navigation and aerospace are continuously growing [12]-[15]. Another important application of NCO is in Digital up conversion and Digital down conversion sub-systems. These sub-system plays a major role in miniaturizing RF system of communication and navigation. Current generation very high speed, high bandwidth DAC/ADC's operating in GHz employs these sub-systems. With the increasing demand and advancement in VLSI design various design methodologies and architectures have been adopted for the design & implementation of NCO for DDFS and DUC-DDC applications. This paper addresses NCO fundamentals, principle and operation, design architectures & their comparisons based on various design parameters. The paper discusses a methodology that can be adopted for design and implementation of NCO on FPGA as per the application requirement. This paper is presented as follows: Section II addresses NCO principle and operation, Section III addresses Design Architectures of NCO and a proposed methodology for its optimum selection, Section IV validates proposed methodology of NCO design for both the applications, Section-V addresses implementation flow of NCO on FPGA. Section VI Concludes with future scope.

2. NCO PRINCIPLE AND OPERATION

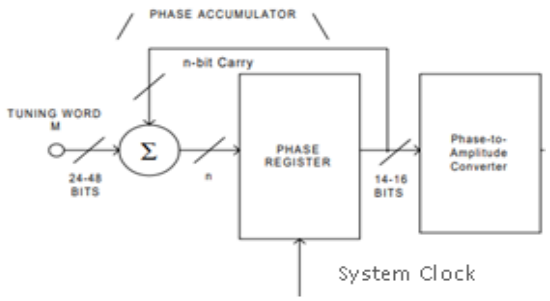

Figure 1 Block Diagram of NCO

NCO: Numerically controlled oscillator is digital means of signal generation usually sinusoidal signal as it is the most commonly used. It is frequency generator which takes stable source frequency (fref) usually square wave as its input and outputs digitized sinusoid signal (fout). As per user requirement the output frequency can be tuned by a frequency control register (FCW) or Tuning word Register. NCO consists of phase accumulator and phase to amplitude converter.
Phase Accumulator: The heart of the system is the phase accumulator whose contents is updated once each clock cycle. Based on the requirement of output frequency resolution accumulator size is decided. For practical applications the accumulator size is in between 24-48 bits. Each time the phase accumulator is updated, the digital number, M (also known as frequency control word (FCW)), is added to the number in the phase accumulator register. For example, initial number is 0 and that the initial contents of the phase accumulator is 0. The phase accumulator is updated by 00...01 on each clock cycle. Thus for accumulator size of 32-bits, 232 clock cycles are required before the phase accumulator returns to 0, and the cycle repeats. Output of the phase accumulator serves as the address used to get amplitude information from phase to amplitude converter..

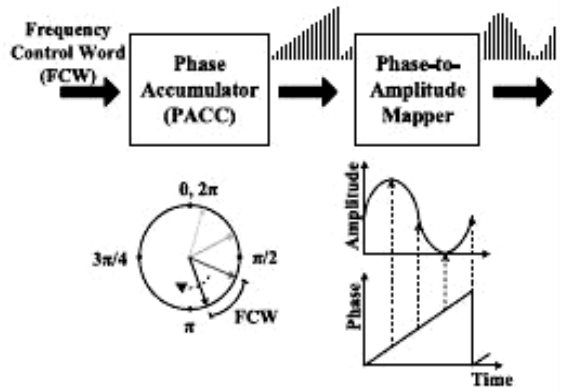

Figure 2 Internal Architecture of NCO

Phase to Amplitude Converter: It contains amplitude information of sine of phase point from phase accumulator. Each address in the lookup table corresponds to a phase point on the sinewave from 0° to 360°. PAC contains the corresponding digital amplitude information for one complete cycle of a sinewave, therefore it maps the phase information from the phase accumulator into a digital amplitude word. The corresponding digital sinewave frequency is equal to the input clock frequency divided by 232.

Frequency tunablity can be achieved using frequency control word, The FCW determines the rate at which phase accumulator register should roll over i.e. M=2 "rolls over" twice as fast, and the output frequency is doubled. This can be generalized as follows as per eq.1

$$f_{out} = \frac{M \times f_{sysclk}}{2^M} \quad (1)$$

3.ARCHITECTURES OF NCO AND A METHODOLOGY FOR ITS OPTIMUM SELECTION FOR AN APPLICATION

There are various methodologies adopted for implementation of NCO and detailed literatures are available focusses on different NCO design parameters and methodology [16]-[32]. However, to the best of our knowledge no paper comprehended all these methodologies in a simpler and effective way considering various NCO parameters and application requirements together. The NCO design and implementation methodology depends on the following parameters based on the user requirement such as precise frequency and phase resolution, FPGA resource utilization/area, power consumption, cost, conversion time, quantization error/spur (frequency domain) and complexity of design. Applications which demands precise frequency control of output frequency, requires phase accumulator with more number of bits, which gives closer phase points however, it demands that many amplitudes corresponding to phases thus increases the area needed for implementation of Phase to Amplitude Converter. Also, higher the resource utilization higher is the power consumption of FPGA. Some application demands smaller conversion time to generate a signal. Conversion time in case of NCO design depends time delays introduced by digital logic of based on the architectures used for Phase accumulator and PAC. Design complexity is also an important parameters a design which is optimum in terms of area, power may not be simple to implement and thus introduces additional time to develop the logic and to test the logic for various test cases/conditions. Thus, there is a trade-off amongst various design parameters of NCO. Thus, selection of most suitable architectures for an optimum NCO design for a particular application is very crucial.
In this section we aim to comprehend various implementation methodologies of NCO design onto

phase accumulator and phase to accumulator conversion logic design and that can be used to design NCO effectively for a particular application.

A) Phase to amplitude conversion logic implementation methodology can be classified as:

1) ROM based LUT design: In this method, amplitude corresponding to phase are stored in look-up table. Here, phase accumulator creates the ROM address and addressing step length is determined by frequency control word. This methodology is simple to implement but at the same, low conversion time, however higher resource consumption.

2) CORDIC (Coordinate Rotation Digital Computer): It is an advance algorithm which calculates trigonometric, exponential and logarithmic functions. It is an iterative operation based approach which requires only shift and addition operation. This method requires very less resource consumption than LUT based approach However, due to its iterative nature conversion time is very high, roughly it takes 16 cycles to compute the sine waveform. Also, complexity of the design is high thus, takes additional design time.

3) Smart ROM based LUT utilizing symmetric property of sinusoidal signal: In this method, resource consumption of PAC in using ROM based LUT approach can be reduced to ¼ or ½ using quarter and half symmetric property respectively. Using quarter/half wave symmetry property only one fourth/half amplitude of sinusoidal signal corresponding to a quarter/half wave will be saved in the LUT and amplitudes for remaining phases will be computed using additional control and computing logic. This approach save resources at the cost of extra logic which increases some complexity to design

4) Phase truncation: The requirement of precise frequency control needs accumulator with higher bit width but this will cause more resource consumption of PAC. In this approach to save resources/area instead of saving amplitude corresponding to all phases only few amplitudes were saved corresponding to reduced number of bits (MSB only) of accumulator, for example accumulator with 32 bits wide with PAC corresponding to P MSB bits (16 bits) i.e. resource requirement of 216 would be needed.

5) Amplitude truncation: The discrete value or amplitude of sine wave corresponding to a particular phase needs to be expressed in finite digital bits. Selection of optimum number of bits will be based on optimization of resource/area and quantization error. Since NCO design is digital means of generating waveform which needs to be converted to analog waveform using Digital to Analog Converter (DAC). There is quantisation error associated with this conversion which causes spurs in the frequency domain at the output of NCO. Based on results of lot of experiments, quantization error improved by 6dB for each additional bit, thus reduces spur. Thus, based on the requirement of spur and resources optimization amplitude truncation can be adopted.

B) Phase Accumulator consists of adder and registers based on size of accumulator various types of adder can be used considering the requirement implementation methodology can be classified as:

1) Serial Adder: Serial adder performs addition operation serially, this topology is simpler to implement, consume least resources however takes N number of cycles to complete the addition. Where N is accumulator size. Thus, utilizing this adder in NCO will have high conversion time.

2) Parallel Adder: Parallel adder performs addition parallel thus, has low conversion time however it employs N number of parallel adders, where N is accumulator size, thus huge resource utilization

3) Pipeline Adder: Pipelining can further reduced the conversion time by adding additional register in between the architecture of parallel adder but at the cost of additional FPGA resources. Various stages of pipelining can be used based on requirement of speed and area.

Thus, based on application requirement out of these mentioned techniques, selection of a particular topology can be adopted for implementation of NCO design on FPGA. Now, case studies of two important applications of NCO i.e. DDFS and DUC/DDC will be addressed, describes the system requirement and topologies that can be used for its effective implementation. Also, additional methods that can be employed to fulfil the overall system requirement.

4. NCO DESIGN FOR ITS APPLICATION USING DISCUSSED METHODOLOGY: DIRECT DIGITAL FREQUENCY SYNTHESIS (DDFS) AND DIGITAL UP CONVERTER/DIGITAL DOWN CONVERTER

An important application of NCO is in direct digital frequency synthesis (DDFS) which generates sinusoidal signal using NCO, which is a digital part implemented in FPGA (Field Programmable Gate

Array) & Digital to Analog Converter with LPF (Low Pass Filter) constituting analog part of it. DDFS can be used in signal generators, communication systems, Satellite Communication, navigation systems etc. Based on our methodology the optimum NCO design would be using utilizing Smart ROM based LUT with quarter wave symmetry property for phase to accumulator design and pipelining adder for phase accumulator design. Additionally since there is a requirement of very low spurs in frequency domain, the same can be achieved using phase truncation & amplitude truncation. Also, additional methods can be employed to remove quantization error and phase truncation error.

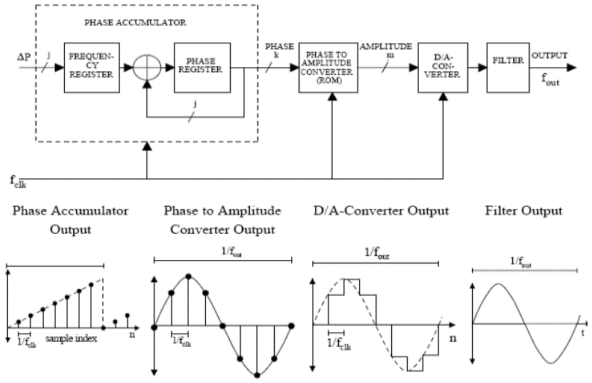

Figure 3 Block Diagram of Direct Digital Frequency Synthesis

In 2019, Sheng Tang.[33] has designed 32 bit DDS on FPGA platform, has implemented NCO in a similar fashion and has focused on spur suppressing method caused by additional quantization in DDS, i.e. additional logic to remove amplitude quantization error using piecewise linear approximation thus reduction in spur.

Another important application of NCO is in digital up converter and digital down converter (DUC/DDC). DUC/DDC sub-systems is very crucial for today's world of technology advancement with very high speed, high bandwidth DAC/ADC's operating in GHz range resulting in low power, small size RF systems of communication and navigation fields. NCO design plays a major role in DUC/DDC sub-system. The methodology discussed above can be utilized for NCO design in this application as following

This application of NCO demands precise frequency and phase control slightest deviation in phase or amplitude of a signal will results in huge deviation at the output frequency, low, power, small area. Thus, for this application of NCO the most optimum methodology suggested as per this paper would be using a CORDIC based algorithm for phase to accumulator conversion logic which is an iterative method thus computes amplitude corresponding to phase accurately with lowest resource utilization of FPGA however due to its iterative nature it has large conversion time. The same can be compensated by designing phase accumulator using pipeline adder with least conversion time. In 2020, Zehua Zhu [34] proposed an NCO design for 16-bit 12GSPS DAC with 48 bit phase accumulator design using 12-stage pipeline adder with each adder of parallel type. Also, phase to accumulator conversion logic was designed using CORDIC algorithm for precise frequency and phase control.

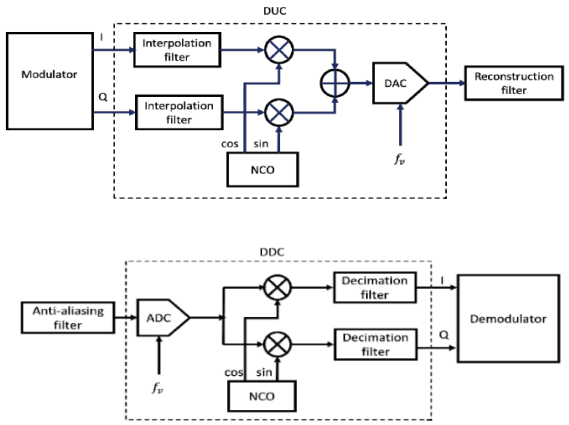

Figure 4 Block Diagram of Digital up converter (DUC) and Digital down converter (DDC)

5. IMPLEMENTATION FLOW

The flow includes specification finalization, behavioral description, RTL description using VHDL or Verilog, functional verification and testing of implemented logic by test-bench creation if in this stage specifications are not met design needs to be optimize for the same. After completion of functional verification, logic synthesis along with timing verification is done results in gate level netlist, this stage also involves logical verification and testing to ensure functional validity on generated netlist, if at this stage design does not meet specification, design needs to be optimized again.

Now based on the proposed optimum selected architecture the same can be implemented by hand-coded register transfer language using HDL language

(VHDL/VERILOG), designed NCO is then simulated to ascertain the targeted specifications are met using Xilinx ISE/Vivado tools, the functionally verified RTL meeting all the required specifications of the application is synthesized and implemented on FPGA as shown in fig 5.

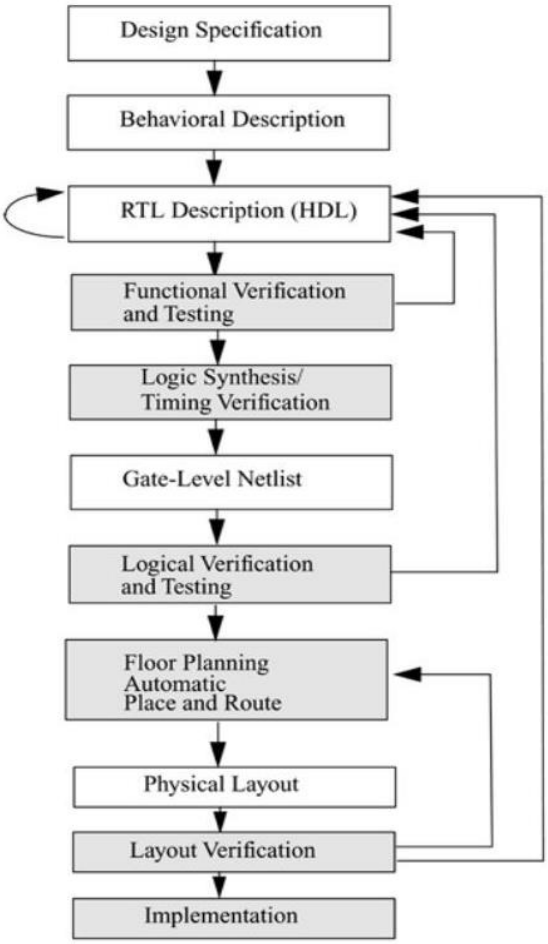

Figure 5 NCO Implementation flow on FPGA

6.Conclusion and future work

In this paper we have comprehend various design methodology of NCO blocks i.e. Phase Accumulator and Phase to Accumulator conversion logic. Thus proposes an effective and simple design methodology considering various NCO design parameters and NCO application requirements together along with their trade-off. The effectiveness of proposed methodology is demonstrated considering NCO design architecture used by researcher for two applications i.e. DDFS (Direct Digital frequency Synthesis) and Digital up converter / Digital down converter. As a future scope, the proposed methodology can be extended for other NCO application incorporating application requirement resulting a generalised methodology that can be used for effective NCO implementation for an application.

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